AHIP5+

Advanced High Integration Platform with Pentium® Processor

P/N 118371-001A

Printed in the United States of America
Part Number 118371-001A

XYCOM
750 North Maple Road
Saline, Michigan 48176-1292
(313) 429-4971

Xycom Revision Record

Revision	*Description*	*Date*
A	Manual Released	5/97

Address comments concerning this manual to:

xycom

Technical Publications Department
750 North Maple Road
Saline, Michigan 48176-1292

Part Number: 118371-001A

Xycom Manual Bug Report

This form is used to track errors that may exist in our manuals and to incorporate improvements. Please describe any errors found in this manual or provide suggestions on how to improve its usefulness. We appreciate your input.

To return this form, fold it in half so the postage-paid* side shows, and tape it closed.

Current Information

Page number(s): _____ Figure number(s): _____

Information as currently printed: _____

_____

_____

Proposed Change(s)

Information as it should be printed: _____

_____

_____

Additional information: _____

_____

_____

Address (optional)

Name _____ Title _____

Company _____

Street Address _____

City _____ State _____ ZIP _____ Phone _____

This box for Xycom use only.

Date Received:

Date Resolved:

Manner Resolved:

PCN #: **Revision:** **Void:**

AHIP5+, Advanced High Integration Platform with Pentium Processor Manual, 118371-001A

**If mailing this card from outside the United Sates, please use an envelope with the appropriate postage.*

Table of Contents

Chapter 2 – Installation (conitnued)

Appendix C – Pinouts (continued)

Chapter 1 – Introduction

Product Overview

The Xycom Advanced High-Integration Platform (AHIP5+) board is designed expressly for use in Xycom's line of flat panel industrial personal computers. The AHIP5+ is optimized in design, layout, and features for use with flat panel computer systems. This integrated design approach allows Xycom industrial PC/ATs to incorporate "Big PC" features in an extremely compact package. These "Big PC" features include "industry first" PCI/ISA expansion, Pentium CPU, full-size hard disk, status LEDs, infrared port, and integrated touchscreen.

Module Features

The AHIP5+ offers the following features:

- Supports
    - 133 MHz, 166 MHz, and 200 MHz Pentium® processors
    - 166MHz and 200 MHz Pentium processors with MMX™
- 8 Mbytes to 64 Mbytes EDO DRAM
- PCI local bus SVGA controller supports
    - Both flat-panel and CRT formats to 1024x768 resolution
    - 2Mbyte video memory
    - Up to 1024x768x256 colors non-interlaced
    - 640x480x256K, 800x600x64K, 1024x768x256 color TFT panels
- PCI fast IDE controller
- Two 16550-compatible serial ports
    - COM 1 is RS-232, or RS-485
    - COM 2 is RS-232 port, or Infrared (IR or IrDA), or Touchscreen
- Centronics-compatible parallel port
- PCI and PC/AT™ expansion
- External floppy connector
- Touchscreen interface (COM 2)
- PS/2 keyboard port
- Real time clock and battery

- LED interface
- Designed specifically for Xycom industrial PC/ATs.

Architecture

This section describes the architecture of the AHIP5+ Pentium processor module.

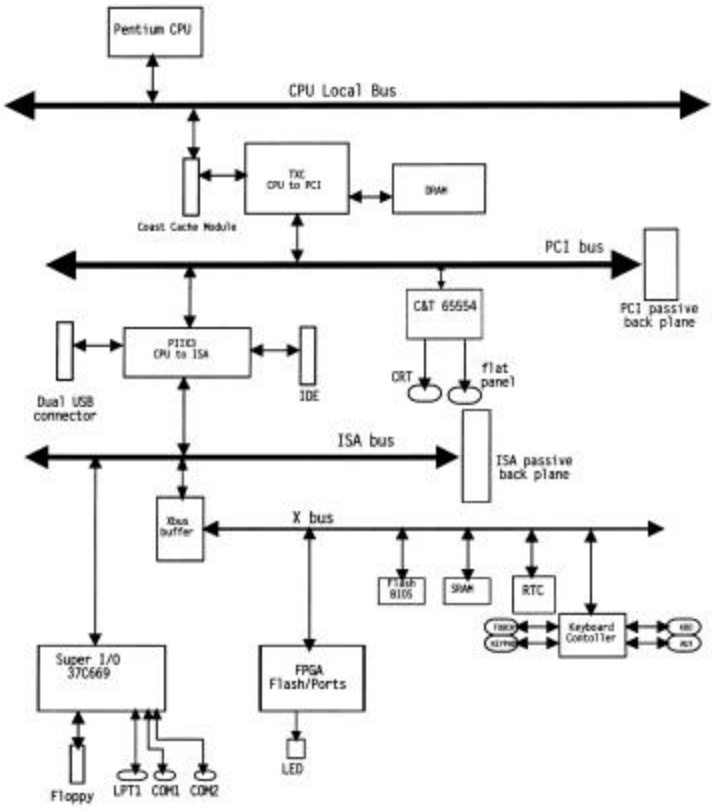

Figure 1- 1. Functional block diagram-AHIP5+

CPU

The AHIP5+ supports the following Intel Pentium CPUs:

- 133 MHz, 166 MHz, and 200 MHz Pentium
- 166 MHz and 200 MHz Pentium with MMX

The secondary cache accommodates COAST rev 3.0 cache modules**.** The COAST module can handle the following cache configurations:

- No cache
- 256K pipeline burst
- 512K pipeline burst

The BIOS and the chipset detect and enable the inserted COAST module.

PCI Local Bus Interface

The Pentium design uses the Triton HX chip set. The Triton HX integrates a high performance interface from PCI to IDE. This interface is capable of accelerated data transfers.

The Triton HX chipset provides an accelerated PCI-to-ISA interface that includes

- A high-performance enhanced IDE controller
- PCI and ISA master/slave interfaces
- Plug-and-play port for on-board devices

The chipset also provides many common I/O functions found in ISA-based PC systems, including

- Seven-channel DMA controller
- Two 82C59 interrupt controllers
- 8254 timer/counter
- Control logic for NMI generation

VGA Graphics Controller

The PCI bus controller supports CRT displays and flat panel displays with 2 Mbyte video memory. The controller also supports resolutions of 640x480, 800x600, and 1024x768 with 64K colors.

Fast IDE controller

The high-speed local bus IDE controller supports programmed I/O (PIO) modes 0-4. It also provides 4x32-bit read-ahead buffer and 4x32-bit write-post buffer support to enhance IDE performance.

Note

The IDE controller supports enhanced PIO modes, which reduce the cycle times for 16-bit data transfers to the hard drive. Check with your drive manual to see if the drive you are using supports these modes. The higher the PIO mode, the shorter the cycle time.

Select the PIO modes in the BIOS setup (refer to Chapter 3). The auto-configure classifies the drive connected if the drive supports the auto ID command. If you experience problems, change the PIO to standard.

Expansion Options

The AHIP5+ offers expansion when used in conjunction with a Xycom Plug-in Expansion Backplane. This gives the user a total of six full length slots:

- Four dedicated ISA slots
- One dedicated PCI slot
- One slot that can be either ISA or PCI

On-board Memory

DRAM

The AHIP5+ has two 72-pin SIMM memory sites, providing up to 64 Mbytes of DRAM. The memory site is populated by standard fast page mode memory or extended data out memory (EDO). EDO memory improves DRAM read performance.

According to an Intel benchmark report, the Triton chipset with no cache and EDO memories competes favorably with chipsets with 256K asynchronous L2 cache.

Flash BIOS

The AHIP5+ board uses a Flash BIOS. Flash is used for system BIOS and video BIOS.

Non-volatile SRAM

The AHIP5+ hardware supports non-volatile SRAM. Contact Xycom at 1-800-AT-XYCOM (1-800-289-9266) for additional information about this feature.

The SRAM comes in a module type package and contains a built-in battery and battery backup circuitry. The battery life is approximately seven years in the absence of VCC. The SRAM supports 32Kx8 and 128Kx8 memory sizes. The RAM comes in a 32 pin dip (0.6 inches wide) standard format.

SRAM can be located at: CC000, D0000, or D8000.

Serial and Parallel Ports

PC/AT peripherals include two high-speed, RS-232C, 16550-compatible serial ports and one bi-directional Centronics-compatible parallel port:

- COM 1 of the serial ports accepts either RS-232 or RS-485 connections.
- COM 2 is RS-232 (stacked DB 25) with parallel port.

The COM2 port can be used for one of three options:

- Serial port out the 25 pin DB connector
- Touchscreen controller interface
- Infrared (IrDA) interface

The BIOS setup is used to configure the port as a serial port or IrDA port. This port can be used as both a serial interface and an IR interface, by allowing software to control the connection.

If the touchscreen controller is jumpered to use COM2, the 25-pin DB connector must not be used to interface to a device. These lines are combined internally. The BIOS setup menu for COM2 must be set to standard operation to use the touch-screen controller on COM2.

Keyboard Interface

The keyboard interface uses a standard PS/2-style connector. A polyswitch protects the +5 V. This device opens if the +5 V is shorted to GND. Once you remove the shorting condition, the polyswitch allows current flow to resume.

Hard and Floppy Drives

The floppy interface supports one floppy drive. The AHIP5+ can interface to a floppy via the on-board floppy connector or the external floppy connector.

In order to connect a floppy drive to the external connector after power up, the floppy drive must be setup for a 1.44 Mbyte drive and the floppy drive test must be disabled. If this is not done the system generates a floppy drive error during the POST (Power On Self Test).

The enhanced IDE (EIDE) interface supports up to 2 hard drives. Hard drive interface is via the Xycom plug-in backplane or the on-board IDE controller.

Caution

The higher the PIO mode, the shorter the cycle time. As the IDE cable length increases, this reduced cycle time can lead to erratic operation. The total IDE cable length must not exceed 18 inches. If two IDE drives are connected, they must not be more than six inches apart.

Environmental Specifications

Table 1- 1. Environmental Specifications

Characteristic	Specification
Temperature	
Operating	0° to 60° C (32° to 140° F)
Non-operating	-40° to 85°C (-40° to 185°F)
Humidity	
Operating	20% to 80% RH non-condensing
Non-operating	20% to 80% RH non-condensing
Altitude	
Operating	Sea level to 10,000 feet (3048 m)
Non-operating	Sea level to 50,000 feet (15240 m)
Vibration* (9465 system **)	
Operating	5 to 55Hz 0.006” peak to peak displacement 56-2000 Hz 1.0g maximum accekeration
Non-operating	5-55 Hz 0.006” peak to peak displacement 56-2000 Hz 2.5 g maximum acceleration
Shock* (9465 system **)	
Operating	15g peak acceleration, 11 msec duration
Non-operating	30g peak acceleration, 11 msec duration

* These values are with solid state hard drives and NOT rotating media drives

** Consistent with system level specifications. See your system manual if you have a system other than the 9465.

Hardware Specifications

Table 1- 2. Hardware Specifications

Characteristic	Specification	
Power Specifications	Typical	Maximum
+12V	90mA	112.5mA
-12V	30mA	37.5mA
+5V		
133MHz	4.0A	5A
166MHz	4.6A	5.75A
200MHz	5.1A	6.38A
200MHz MMX	5.7A	7.125A
CPU speed	133 MHz, 166 MHz, or 200 MHz	
PCI Super VGA Graphics Controller	640x480, 800x600, and 1024x768, 64K colors maximum resolution 2 Mbyte video DRAM	
Serial Ports (2)	COM1 is RS-232 or RS-485 COM2 is RS-232, or IR, or Touchscreen Both 16550 compatible	
Parallel Interface	Centronics compatible	
On-board memory	Up to 64 Mbytes DRAM	

Chapter 2 – Installation

This chapter provides information on configuring the AHIP5+ Processor Module. Pinouts for the connectors are located in Appendix C.

Figure Chapter 2 -1 illustrates the jumper and connector locations on the AHIP5+.

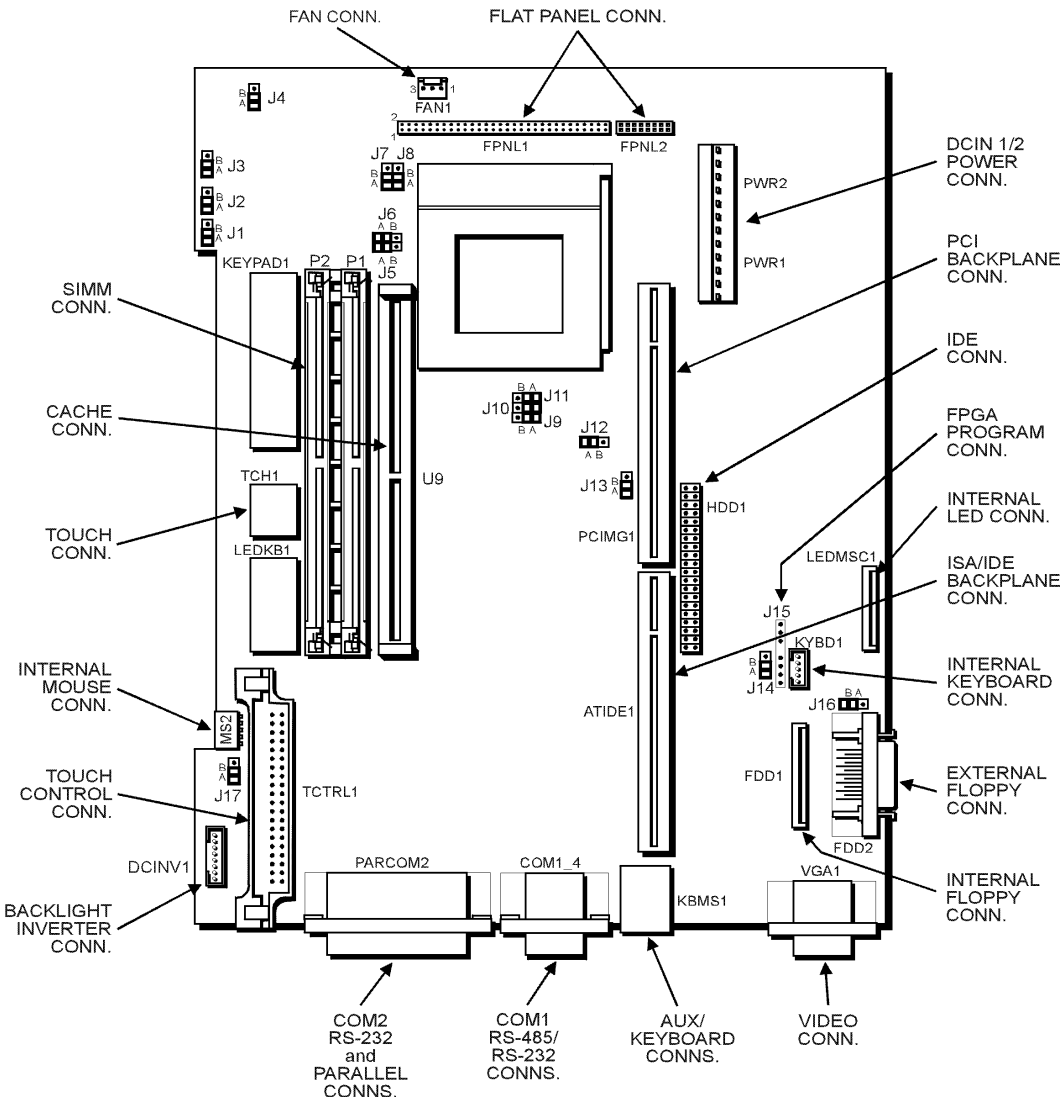

Figure Chapter 2 -1. AHIP5+ Jumper and Connector Locations

Configuration Options

Jumper Settings

Table Chapter 2 -1 lists AHIP5+ jumpers, their default positions and their functions. The jumpers marked *Access* are at the top of the board for easy customer access.

Table Chapter 2 -1. AHIP5+ Jumpers

Jumper	Position	Function
J1	A	Push button reset switch DISABLED (Access)
	B	Push button reset switch ENABLED
J2	A	CMOS OK (Access)
	B	Clear CMOS
J3	A	Flat panel selected (Access)
	B	CRT selected
J4	A	Internal keyboard controller ROM
	B	External keyboard ROM
J6, J5	A	5V memory
	B	3.3V memory
J8, J7	B B B A A B A A	166 MHz 200 MHz 133MHz 100MHz
J9 - J12	A	CPU core voltage is 3.45V
	B	CPU core voltage is 2.8V. Used for MMX processors
J13	A	VGA ENABLED (Access)
	B	VGA DISABLED
J14	A	Boot flash enabled
	B	AT Boot enabled
J16	A	Orb ground not connected to logic ground
	B	Orb ground connected to logic ground
J17	A	Normal flash boot
	B	Recovery flash boot

System Interrupts

Table Chapter 2 -2 describes the interrupts used on the AHIP5+.

Table Chapter 2 -2. System Interrupts

Interrupt	Function
IRQ0	System Timer
IRQ1	Keyboard
IRQ2	Cascade
IRQ3	Serial Port*
IRQ4	Serial Port*
IRQ5	Parallel Port*
IRQ6	Floppy Controller
IRQ7	Parallel Port*
IRQ8	Real Time Clock
IRQ9	Unused
IRQ10	Serial Port*
IRQ11	Serial Port*
IRQ12	Mouse Port
IRQ13	Math Co
IRQ14	Fixed Disk
IRQ15	Unused

* BIOS setup controlled

The BIOS setup menu controls the interrupts for the serial and the parallel port.

The 2 Serial ports on the AHIP5+ board can be mapped to any two of the following interrupts 3, 4, 10, & 11. The defaults are interrupts 3 and 4. This would leave IRQ10 and IRQ11 unused. The one parallel port can be mapped to IRQ5 or IRQ7. Use the BIOS setup menu to control the location and interrupts for the serial port and the parallel port.

Note

The BIOS controls the mapping of the PCI interrupts to AT-bus interrupts. This means if a PCI device is plugged into a slot and needs an interrupt, one of the AT-bus interrupts must be mapped to the PCI interrupt.

DMA Mapping

Table Chapter 2 -3. DMA Channels

DMA	Function
DMA0	Unused (Could be used for EPP/ECP parallel port option)
DMA1	Unused
DMA2	Floppy Controller
DMA3	Unused (Could be used for EPP/ECP parallel port option)
DMA5	Unused
DMA6	Unused
DMA7	Unused

The DMA channels 0-3 are 8-bit, DMA channels 5-7 are 16-bit. When the ECP option is enabled one of the 8-bit DMA channels is used.

Memory Map

Table Chapter 2 -4 shows the AHIP5+ memory map. The I/O designation refers to memory viewed as part of the AT bus.

Table Chapter 2 -4. Memory Map

Address Range (HEX)	Size	Device
FFFE0000 - FFFFFFFF	128K	SYSTEM BIOS
end of DRAM - FFFDFFFF	xxxK	I/O Memory
00100000 - end of DRAM	xxxK	DRAM (Maximum on-board DRAM)
000F0000 - 000FFFFF	64K	SYSTEM BIOS
000E0000 - 000EFFFF	64K	SYSTEM BIOS
000D0000 - 000DFFFF	64K	AT bus I/O
000C0000 - 000CBFFF	48K	VGA BIOS
000A0000 - 000BFFFF	128K	VGA DRAM MEMORY
00000000 - 0009FFFF	640K	DRAM

I/O Map

The I/O map for the AHIP5+ in Table Chapter 2 -5 contains all the I/O ports of the IBM AT architecture with some additions.

Table Chapter 2 -5. I/O Map

Hex Range	Device
000-01F	DMA controller 1, 8237A-5 equivalent
020-021	Interrupt controller 1, 8259 equivalent
022-024	Available
025-02F	Interrupt controller 1, 8259 equivalent
040-05F	Timer, 8254-2 equivalent
060-06F	8742 equivalent (keyboard)
070-07F	Real Time Clock bit 7 NMI mask
080-091	DMA page register
092	Reset/ Fast Gate A20
93-9F	DMA page register
0A0-0BF	Interrupt controller 2, 8259 equivalent
0C0-0DF	DMA controller 2, 8237A-5 equivalent
0F0	N/A
0F1	N/A
0F2-0F3	N/A
0F4	IDE ID port
0F5-0F7	N/A
0F8	IDE Index port
0F9-0FB	N/A
0FC	IDE Data port
0FD-0FF	N/A
100	Available
102	C&T Global enable register
103-179	Available
180-181	SRAM control register (May be remapped based on I/O port 234h)
182-1EF	Available
1F0-1F7	IDE Controller (AT Drive)
1F8-22F	Available

Hex Range	Device
231	Xycom LED port
233	Xycom Flash control register
234	Xycom IO port control register
278-27F	Parallel Port 2
280-2F7	Available
2F8-2FF	Serial Port 2
300-36F	Available
370-377	Alt. Floppy Disk Controller
378-37F	Parallel Port 1
380-3AF	Available
3B0-3BB	mono mode video
3BC-3BF	reserved for parallel port
3C0-3CF	VGA registers
3D0-3DF	CHIPS flat panel & color mode registers
3E0-3EF	Available
3F0-3F7	Primary Floppy disk controller
3F8-3FF	Serial port 1
CF8	PCI configuration address register
CFC	PCI configuration data register

Note

Serial and parallel port addresses are controlled in the BIOS Setup Menu. Changing the setting will change the I/O location.

Note

Serial and parallel port interrupts are available if software does not use the ports or does not use the interrupt.

Registers

The AHIP5+ contains three ports: 231h, 233h, and 234h.

Register 231h – CPU LED Port

Register 231h controls the LEDs and signals shown in Table Chapter 2 -6.

Table Chapter 2 -6. Register 231h - CPU LED Port

Bit	LED/Signal	Result	R/W
0	Reserved	0	R
1	Reserved	0	R
2	Reserved	0	R
3	Reserved	0	R
4	Reserved	0	R
5	ENFLASHWR	1 = Enables Flash write*	R/W
6	VGA_EN	1 = Enables on-board VGA	R
7	CLRCMS	1 = CMOS okay 0 = Clear CMOS	R

*Note: This bit must be 1 to make FLASH visible at D0000h when booting from AT bus.

Register 233h – Flash BIOS Control

Register 233h controls the signals shown in Table Chapter 2 -7.

Table Chapter 2 -7. Register 233h - Flash BIOS Control Register

Bit	Signal	Result	R/W
0	FLA15	Flash address 15 - page control bit	R/W
1	FLA16	Flash address 16- page control bit	R/W
2	FLA17	Flash address 17 - page control bit	R/W
3	FLA18	Flash address 18 - page control bit	R/W
4	FPSEL0	Flat panel select bit 0	R
5	FPSEL1	Flat panel select bit 1	R
6	FPSEL2	Flat panel select bit 2	R
7	FPSEL3	Flat panel select bit 3	R

Register 234h - I/O Port Location

Register 234h controls the I/O port location register shown in Table Chapter 2 -8.

Table Chapter 2 -8. Register 234h - I/O Port Location Register

Bit	Signal	Result	R/W
0	Reset	Low to reset interface or disable transmission	R
1	Write data bit	Write data	R
2	Read data bit	Read data	R
3	CLK bit	Clock	R
4	i/O range select	I/O range select bit 0	R
5	I/O range select	I/O range select bit 1	R
6	I/O port bit0	I/O port bit 0	R/W
7	I/O port bit1	I/O port bit 1	R/W

Bits 0-3 are reserved for the temperature sensor. Bits 4 and 5 are reserved for setting the memory location for the SRAM.

I/O Range Select

The following are ranges defined by register 234h.

Table Chapter 2 -9. I/O Range Selection

I/O range selection	Range
00	no range
01	CC000-CFFFF
10	D0000-D7FFF
11	D8000-DFFFF

Offset Registers

The following registers are located starting at the I/O location defined by register 234h, bits 6 and 7.

Table Chapter 2 -10. I/O Port Selection (Port Address)

I/O port selection	Port address
00	180h
01	2E0h
10	3E0h
11	300h

Offset 0 Page Register for Programming (Port Address)

Offset 0 is a read-only register that checks the battery status

Table Chapter 2 -11. Offset 0 Page Register for Programming (Port Address)

Bit	Signal	Result	R/W
0	Battery status	0 = battery good 1 = battery fail	R
1	Reserved	0	R
2	Reserved	0	R
3	Reserved	0	R
4	Reserved	0	R
5	Reserved	0	R
6	Reserved	0	R
7	Reserved	0	R

Offset 1 Page Register for Programming (Port Address +1)

Offset 1 controls the paging bits for the ROM. This feature is needed for programming flash.

Table Chapter 2 -12. Offset 1 Page Register for Programming (Port Address +1)

Bit	Signal	Result	R/W
0	Control ROM/RAM15	ROM address 15-page control bit	R/W
1	Control ROM/RAM16	ROM address 16-page control bit	R/W
2	Control ROM/RAM17	ROM address 17-page control bit	R/W
3	Reserved	0	R
4	Reserved	0	R
5	Reserved	0	R
6	Reserved	0	R
7	Reserved	0	R

Connectors

This section describes the connectors for the AHIP5+. Appendix C provides the pinouts for each of the connectors.

Parallel Port Connector (PARCOM2)

The parallel port is a stacked 25 pin dB.

NOTE: In Appendix C, the suffix “A” denotes the lower connector which is the LPT1 port.

Serial Port Connectors

There are two serial ports supported on the AHIP5+ board.

COM1 Connector (COM1)

The COM1 connector actually consists of two connectors attached to one logical port. Only one connector can be used at a time, either the RS-232 port or the RS-485 port.

COM1 is a nine-pin connector.

In Appendix C, the suffix ‘A’ denotes the lower connector (RS-232) and the suffix ‘B’ denotes the upper connector (RS-485).

COM2 Connector (PARCOM2)

The second serial port, COM2, is connected to a 25 pin dB that sits on top of the parallel port.

COM2 can be used for 3 separate devices but only one at a time. The COM2 port can be used for the touchscreen controller, the infrared (IR, IrDA) interface or the RS-232 connector. The BIOS setup determines whether the COM2 is used for the RS-232 connector or the IR interface. Jumpers on the touchscreen controller select the COM2 port or the auxiliary port. If a touchscreen controller is jumpered for COM2, this COM port is not available.

In Appendix C, ‘B’ denotes the upper COM2, RS-232, port.

This connector also contains the remote system reset option. A normally open push button switch can be connected to pins 11B and 7B. When the switch is pressed the PB_RESET* signal is forced to GND, which causes the CPU to reset. For this option to be enabled, J1 must be in position B.

PS/2 Keyboard Port Connector (KBMS1)

This double stacked connector provides an upper and lower connector for the keyboard and auxiliary port.

The keyboard connector is the lower six-pin connector. This port uses a polyswitch to protect VCC from direct shorts to GND.

Internal Keyboard Connector (KYBD1)

This is a five pin internal keyboard connector on the motherboard.

PS/2 Auxiliary Port Connector (KBMS1)

The auxiliary port is provided for expansion to an integral panel-mounted mouse.

The auxiliary port is the upper six pin connector of the double stacked connector. This port uses a polyswitch to protect VCC from direct shorts to GND.

If the touchscreen controller is using the auxiliary port, this interface is not available. If the touchscreen is factory-installed the unit is shipped with a label covering this port.

VGA Connector (VGA1)

The VGA(Video) connector is a 15-pin connector located on the I/O panel. This connector is only enabled when J3 is in position B or no flat panel is connected to the CPU board.

Floppy Drive Connector (FDD1 and FDD2)

There is an internal floppy connector (FDD1) and an external floppy connector (FDD2). The floppy interface supports only one floppy drive. The floppy drive connector is a 26-pin connector. Both of these ports use a polyswitch to protect VCC from directly shorting to GND.

Internal Mouse Connector (MS2)

This four-pin connector provides a future method to integrate a mouse to the front panel.

Internal LED Connector (LEDMSC1)

This connector provides a low cost method to add LED's to the touch only units. This 20-pin connector also provides the pinout for the IR interface port.

FPGA Program Connector (J15)

This eight-pin connector is used to program the lattice FPGA. This pinout matches the standard lattice pinout.

ISA/IDE Backplane Connector (ATIDE1)

The ISA/IDE Backplane connector is a 120-pin connector. This connector provides both ISA and IDE signals to the backplane.

IDE Connector (HDD1)

IDE hard drive connector is a 40-pin header. This header is intended for future options and testing.

PCI Backplane Connector (PCIMG1)

PCI backplane connector is a 120-pin connector.

DCIN1 and DCIN2 Power Connectors (PWR1 and PWR2)

The DCIN1 and the DCIN2 are six-pin connectors. Together the DCIN1 and DCIN2 connectors accept a standard PS/2 type PC power supply connector.

Touch Control Connector (TCTRL1)

This 40 pin connector is used for the touchscreen controller. The connector is latching to provide for a DRAM SIMM type installation.

Touch Connector (TCH1)

The five-pin touch connector is the interface to the touch panel.

Flat Panel Connector (FPNL1)

The flat panel connector is a 60pin SMD through board connector. The four flat panel select lines define up to 16 unique panel types. If all signals are high (no cable attached) the system will default to CRT.

The system board supports +5V and 3.3V TFT panels with a custom flat cable. It supports STN panels with a 2.5" X 2.75" PCB which contains the DC/DC for the custom VEE voltage along with the contrast and power sequencing circuit. There are also provisions to support a temperature sensor for automatic contrast control.

Backlight Inverter Connector (DCINV1)

This 8-pin connector provides power for the backlight inverter.

Caution

Do not use excessive force or pressure to engage the connectors.

Chapter 3 – BIOS Setup Menus

The AHIP5+ board's customized BIOS has been designed to surpass the functionality provided for normal PC/ATs. This custom BIOS allows you to access the value-added features on the AHIP5+ module without interfacing to the hardware directly.

Moving through the Menus

General instructions for navigating through the screens are described below:

Key	Result
F1 or ALT-H	General Help window
F2	Enters the menu
ESC	Exits the menu
← or → arrow keys	Selects a different menu
↑ or ↓ arrow keys	Moves the cursor up or down
TAB or SHIFT + TAB	Cycles the cursor up or down
HOME or END	Moves the cursor to the top or bottom of the window
PGUP or PGDN	Moves the cursor to the next or previous page
F5 or -	Selects the previous value for the field
F6 or + or SPACE	Selects the next value for the field
F9	Loads the default configuration values for the menu
F10	Loads the previous configuration values for the menu
ENTER	Executes the Command or Select » Sub-menu
ALT-R	Refresh screen

To select an item, use the arrow keys to move the cursor to the field you want. Then use the + and - keys to select a value for that field. The Save Changes commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub-menu, use the arrow keys to move the cursor to the sub-menu you want. Then press ENTER. A "**»**" indicates a sub-menu.

BIOS Main Setup Menu

Follow the instructions below to start the BIOS Setup utility.

- If the setup prompt is disabled on your system–which is the default– press F2 after the memory tests and before your system loads the operating system to access the main menu.
- If the setup prompt is enabled on your system, the BIOS displays the following message: "Press F2 to enter Setup." Once this message appears, press F2 to access the main menu.

```
          PhoenixBIOS Setup–Copyright 1985-95 Phoenix Technologies Ltd.

    Main      Advanced     Security     Power     Exit

                                                          Item Specific Help

 System Time:             [16:19:20]

 System Date:             [03/02/95]

 Diskette A:              [1.44 MB, 3½"]                  If the line item you
»IDE Adapter 0 Master     (C: 260 Mb)                     are viewing has
»IDE Adapter 0 Slave      (D:105 Mb)                      specific help, it
                                                          will
 Video System:            [EGA/VGA]                       be listed here.
»Memory Cache
»Memory Shadow
»Boot sequence:          [A: then C:]
»Numlock:                [Auto]

 System Memory:           640 KB
 Extended Memory:           7 MB

F1  Help      ↑↓  Select Item     -/+  Change Values      F9  Setup Defaults

ESC Exit      ←→  Select Menu     Enter Select » Sub-     F10 Previous Val-
                                  Menu                    ues
```

Figure Chapter 3 -1. Main Setup Menu

Table Chapter 3 -1 describes the BIOS Main Menu options.

Table Chapter 3 -1. Main Setup Menu Options

Option	Description
System Time (HH/MM/SS)	Sets the real-time clock for hour, minute, and seconds. The hour is calculated according to a 24-hour military clock (i.e., 00:00:00 through 23:59:59). Use TAB to move right; SHIFT + TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to enter the seconds or type zeros in front of numbers.
System Date (MM:DD:YYYY)	Sets the real-time clock for the month, day, and year. Use TAB to move right; SHIFT + TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to type zeros in front of numbers.
Diskette A or B	Selects the floppy-disk drive installed in your system.
Video System	Selects the default video device.
System Memory	Displays the amount of conventional memory detected during boot-up. This field is not user configurable.
Extended Memory	Displays the amount of extended memory detected during boot-up. This field is not user configurable.

IDE Adapter 0 Master and Slave Sub-menu

The IDE Adapter 0 Master and Slave sub-menus are used to configure IDE hard drive information. If only one drive is attached to the IDE adapter, then only the parameters in the Master Sub-menu need to be entered. If two drives are connected, both Master and Slave Sub-menu parameters will need to be entered. The Master and Slave sub-menus contain the same information.

```
            PhoenixBIOS Setup–Copyright 1985-95 Phoenix Technologies Ltd.
      Main
IDE Adapter 0 Master (C: 850 Mb)                    Item Specific Help

Autotype Fixed Disk:      [Press Enter]

Type:                     [User] 850 Mb
Cylinders:                [1647]                    If the line item you
Heads:                    [   16]                   are viewing has
Sectors/Track:            [   63]                   specific help, it
                                                    will
Write Precomp:            [None]                    be listed here.

Multi-Sector Transfers:   [8 Sectors]
LBA Mode Control:         [Enabled]
32 Bit I/O:               [Disabled]
Transfer Mode:            [Standard]

F1  Help      ↑↓  Select Item     -/+  Change Values     F9  Setup Defaults

ESC Exit      ←→  Select Menu     Enter Select » Sub-    F10 Previous Val-
                                  Menu                   ues
```

Figure Chapter 3 -2. IDE Adapter Sub-menu

Table Chapter 3 -2 describes the IDE Adapter Sub-menu options.

Table Chapter 3 -2. IDE Adapter Sub-menu Options

Option	Description
Autotype Fixed Disk	Reads the hard disk parameters from the drive if you press ENTER. Do not attempt to manually set the disk drive parameters unless instructed to do so by Xycom Application Engineering.
Type	Options include 1 to 39, User, or Auto. The 1 to 39 option fills in all remaining fields with values for predefined disk type. “User” prompts you to fill in remaining fields. “Auto” autotypes at each boot, displays settings in setup menus, and does not allow you to edit the remaining fields.
Cylinders	Indicates the number of cylinders on the hard drive. This information is automatically entered if the Autotype Fixed Disk option is set.
Heads	Indicates the number of read/write heads on the hard drive. This information is automatically entered if the Autotype Fixed Disk option is set.
Sectors/Track	Indicates the number of sectors per track on the hard drive. This information is automatically entered if the Autotype Fixed Disk option is set.
Write Precomp	This value is not used or required by IDE hard drives.
Multi-Sector Transfers	Sets the number of sectors per block. Options are Auto, 2, 4, 8, or 16 sectors. “Auto” sets the number of sectors per block to the highest number supported by the drive.
LBA Mode Control	Enables Logical Block Access. The default is disabled and should work with most hard drives.
32-Bit I/O	Enables 32-bit communication between CPU and IDE interface.
Transfer Mode	Selects the method for transferring the data between the hard disk and system memory. Available options are determined by the drive type and cable length.

Memory Cache Sub-menu

Enabling cache increases CPU performance by holding data most recently accessed in a special high-speed static RAM area called cache. The AHIP5+ provides two levels of cache memory; level one is 16 Kbytes internal to the Pentium processor, and level two, or external cache, is the cache-on-a-stick site (COAST) which can accommodate 256 or 512 Kbytes of high-speed cache memory.

```
          PhoenixBIOS Setup–Copyright 1985-95 Phoenix Technologies Ltd.
     Main
Memory Cache                                        Item Specific Help

External Cache:           [Enabled]
Cache System BIOS area:   [Enabled]
Cache Video BIOS area:    [Enabled]                 If the line item you
                                                    are viewing has
Cache Memory Region                                 specific help, it
                                                    will
    CC00-CFFF:            [Disabled]                be listed here.
    D000-D3FF:            [Disabled]
    D400-D7FF:            [Disabled]
    DC00-DFFF:            [Disabled]

F1  Help     ↑↓  Select Item     -/+  Change Values     F9  Setup Defaults
ESC Exit     ←→  Select Menu     Enter Select » Sub-    F10 Previous Val-
                                 Menu                   ues
```

Figure Chapter 3 -3. Memory Cache Sub-menu

Table Chapter 3 -3 describes the available options on the Memory Cache Sub-menu.

Table Chapter 3 -3. Memory Cache Sub-menu Options

Option	Description
External Cache	Controls the state of external (COAST) cache memory. The system BIOS automatically disables external cache if it is not installed. The default is enabled.
Cache System BIOS Area	Allows the system BIOS memory area to be cached if enabled. Enabling also increases system performance. The default is enabled.
Cache Video BIOS Area	Allows the video BIOS memory area to be cached if enabled. Enabling also increases system performance. The default is enabled.
Cache Memory Region	Caches the corresponding memory when enabled. Memory in this area is usually extended BIOS or AT-bus memory. Enabling cache may increase system performance, depending on how the extended BIOS is accessed. The default is disabled.

Memory Shadow Sub-menu

The summary screen displays the amount of shadow memory in use. Shadow memory is used to copy system and/or video BIOS into RAM to improve performance. The AHIP5+ displays the number of Kbytes allocated to Shadow RAM on the summary screen. The System Shadow field, which is not editable, is for reference only.

The AHIP5+ is shipped with both the system BIOS and video BIOS shadowed.

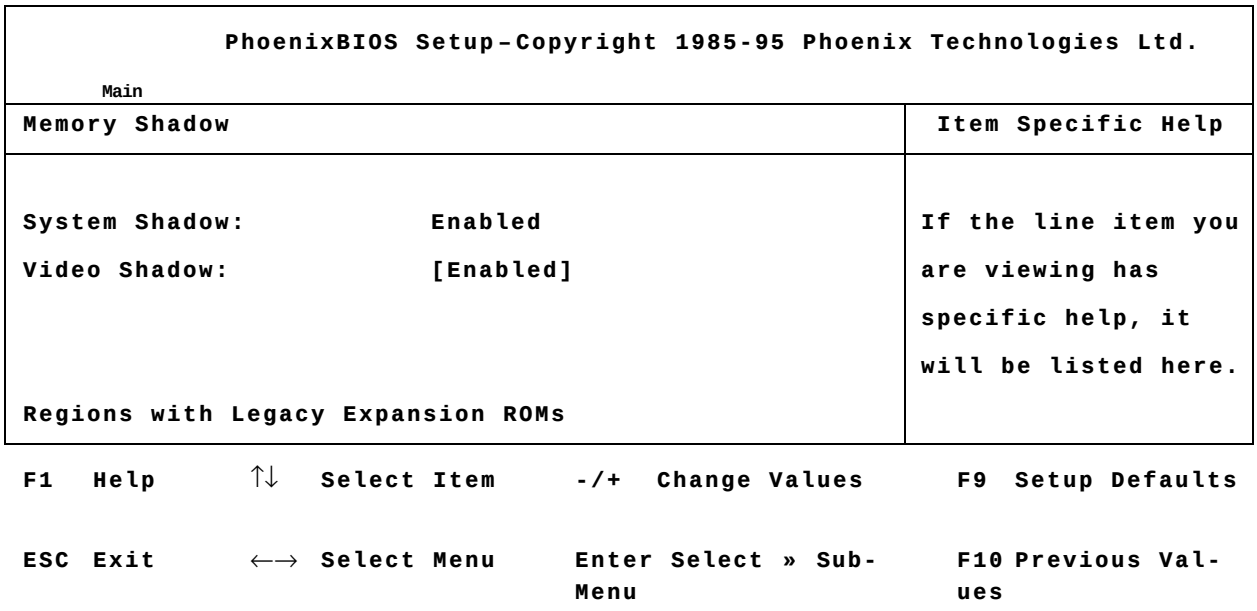

Figure Chapter 3 -4. Memory Shadow Sub-menu

Table Chapter 3 -4 describes the available options on the Memory Shadow Cub-menu.

Table Chapter 3 -4. Memory Shadow Sub-menu Options

Option	Description
System Shadow	Permanently enabled.
Video Shadow	Shadows the video BIOS to improve system performance.
Regions with Legacy Expansion ROMs	Regions are listed below the header if detected by the BIOS

Boot Sequence Sub-menu

This menu allows the boot sequence to be configured.

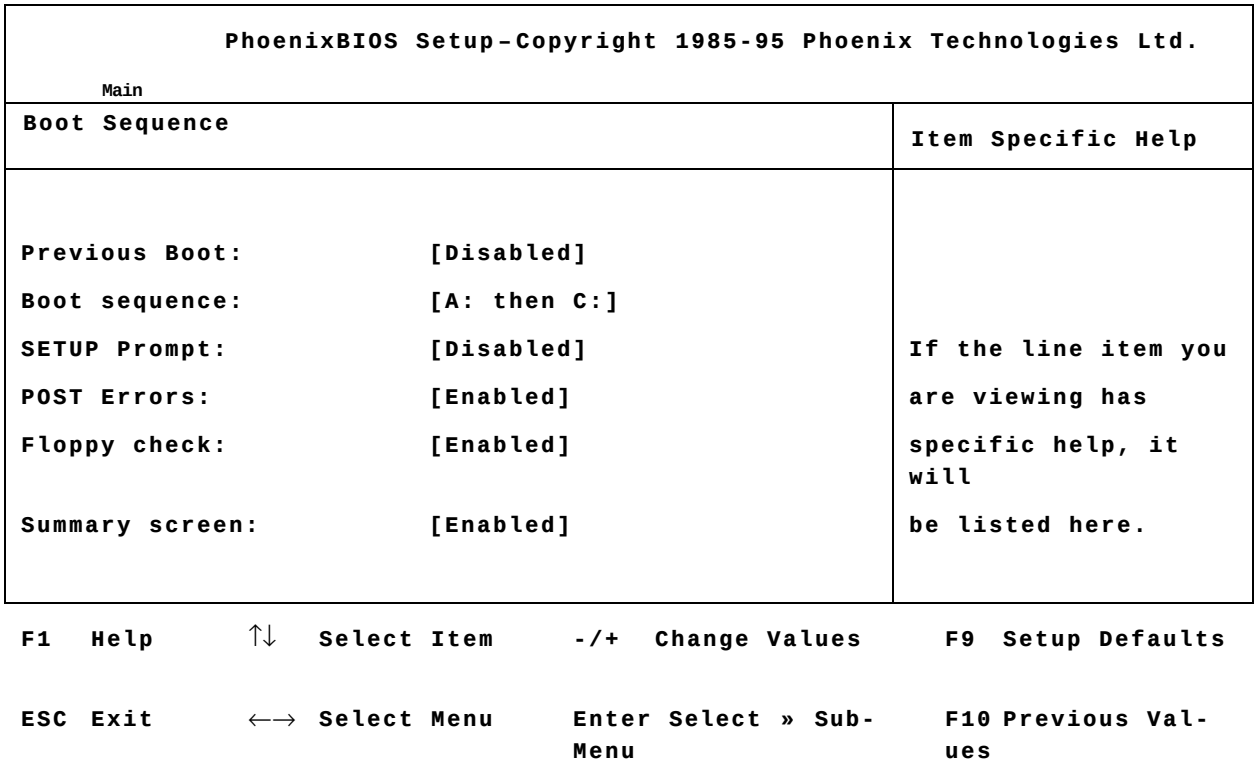

Figure Chapter 3 -5. Boot Sequence Sub-menu

Table Chapter 3 -5 describes the Boot Sequence Sub-menu options.

Table Chapter 3 -5. Boot Sequence Sub-menu Options

Option	Description
Previous Boot	Detects if a boot sequence was not completed properly, if enabled. An incomplete boot may be caused by a power failure, reset during boot-up, or invalid CMOS configuration. If the BIOS detects this condition, it will display the following message: "Previous boot incomplete - default configuration used." The system will be rebooted using the default configuration. If this option is disabled, the system BIOS will not detect an incomplete boot. As a result, the system may not boot if the CMOS settings are wrong. The default is disabled.
Boot Sequence	Attempts to load the operating system from the disk drives in the sequence selected here. The default is A: then C:
Setup Prompt	Displays the message, "Press <F2> for Setup," during boot up. The default is disabled.
POST Errors	Halts the system if it encounters a boot error when enabled, and will display "Press <F1> to resume, <F2> for Setup." The default is enabled.
Floppy Check	Seeks diskette drives on the system during boot up if enabled. Disabling speeds boot time. The default is enabled.
Summary Screen	Displays system summary screen during boot up, when enabled. The default is enabled. This screen is a standard Phoenix BIOS screen and provides information on the following items: Processor Type Coprocessor Type BIOS Date System ROM Address System RAM Extended RAM Shadow RAM Cache RAM COM Ports LPT Ports Display Type Hard Disk 0 Hard Disk 1 Diskette A Diskette B

Numlock Sub-menu

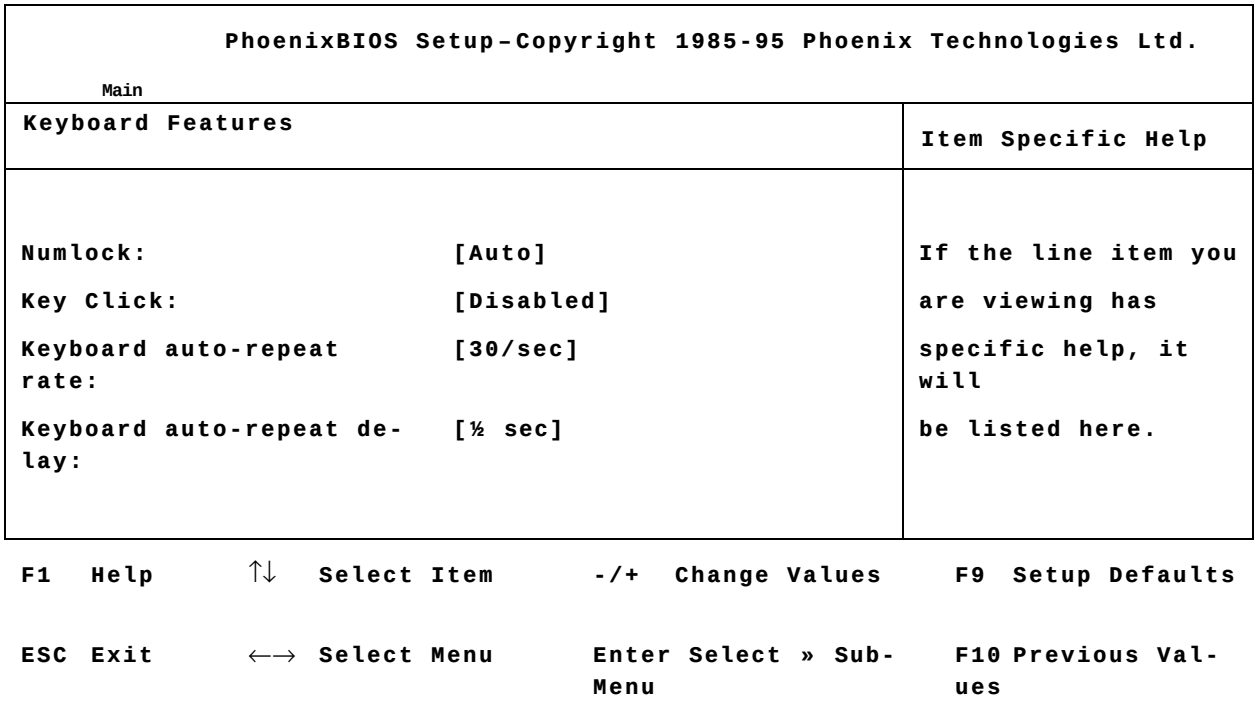

Figure Chapter 3 -6. Numlock Sub-menu

Table Chapter 3 -6 describes the Numlock Sub-menu options.

Table Chapter 3 -6. Numlock Sub-menu Options

Option	Description
Numlock	Determines how the BIOS defines the numlock key at power up or soft reset. Normally, the BIOS sets the numlock (numeric keys selected) if it detects a 101- or 102-key keyboard at power up. If an 84-key keyboard is detected, numlock is turned off (cursor keys selected). Select “Auto” to keep this state; “On” to select the numeric keys, regardless of keyboard; or ”Off” to select the cursor keys, regardless of keyboard. The default is Auto.
Keyboard click	Provides audible key-press feedback by causing the BIOS to click through the system speaker every time a key is pressed, if enabled. This option is only valid for systems with a speaker connected to the speaker jack. The default is disabled.
Keyboard auto-repeat rate	Defines the rate at which the keyboard repeats while a key is pressed. The higher the number, the faster the key repeats. The default is 30 times per second.
Keyboard auto-repeat delay	Sets the delay time after a key is held down, before it begins to repeat the keystroke. The default is a ½ second.

Advanced Menu

This menu allows you to change the peripheral control, advanced chipset control, and disk access mode.

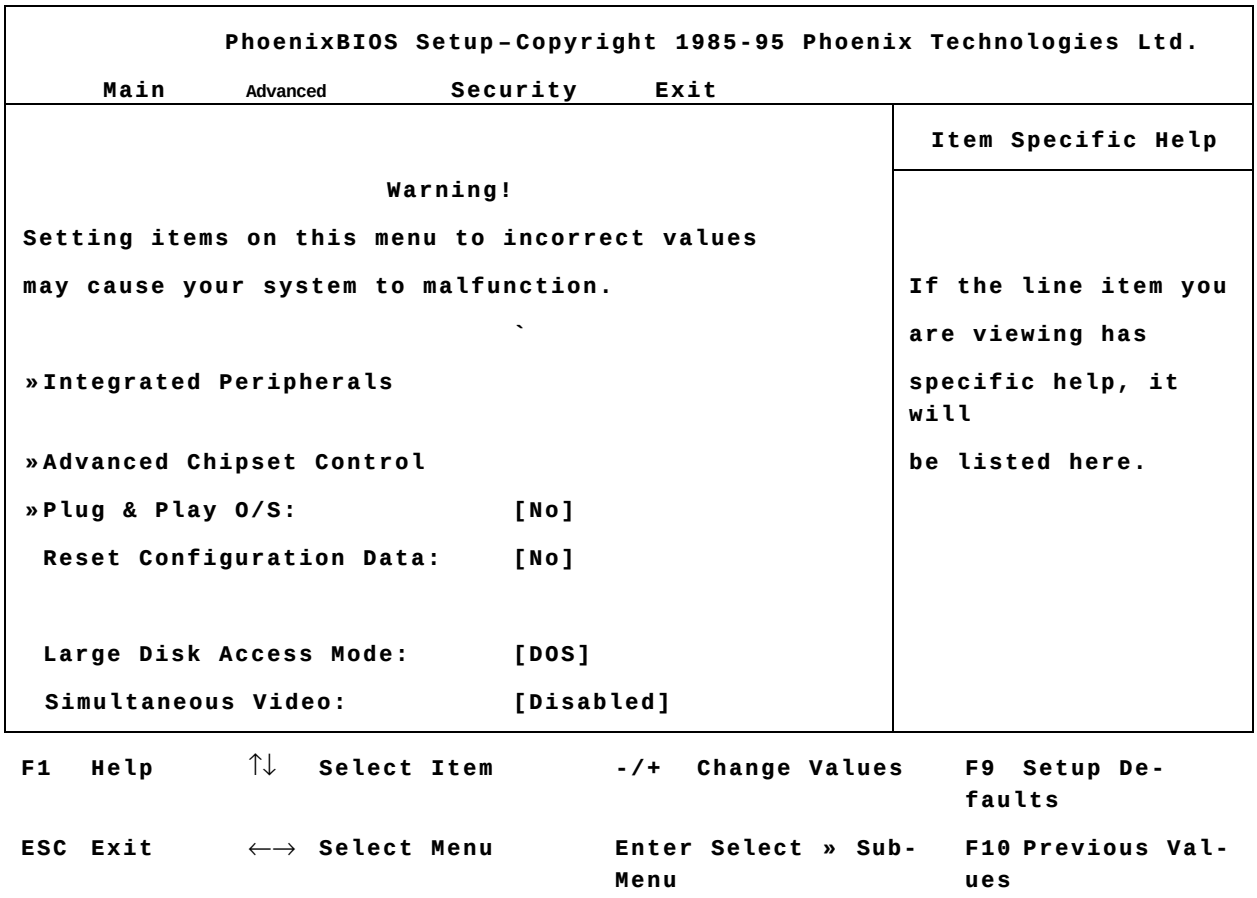

Figure Chapter 3 -7. Advanced Setup Menu

Table Chapter 3 -7. Advanced Menu Option

Feature	Description
Plug & Play O/S	Select "Yes" if you are using an operating system with Plug & Play capabilities.
Reset Configuration Data	Used to reset the Plug & Play configuration data table when new devices are added/removed or whenever the BIOS is upgraded.
Large Disk Mode	Select “DOS” if your system has DOS. Select “Other” if you have another operating system, such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads, or more than 63 tracks per sector.
Simultaneous Video	Select “Enabled” if you want both a video display out the CRT port and the flat panel display. Note: Only available with TFT flat panels Select “Disabled” if you want only the flat panel display.

Integrated Peripherals Sub-menu

The Integrated Peripherals Sub-menu is used to configure the COM ports, parallel ports, and enable/disable the diskette and enhanced IDE controllers.

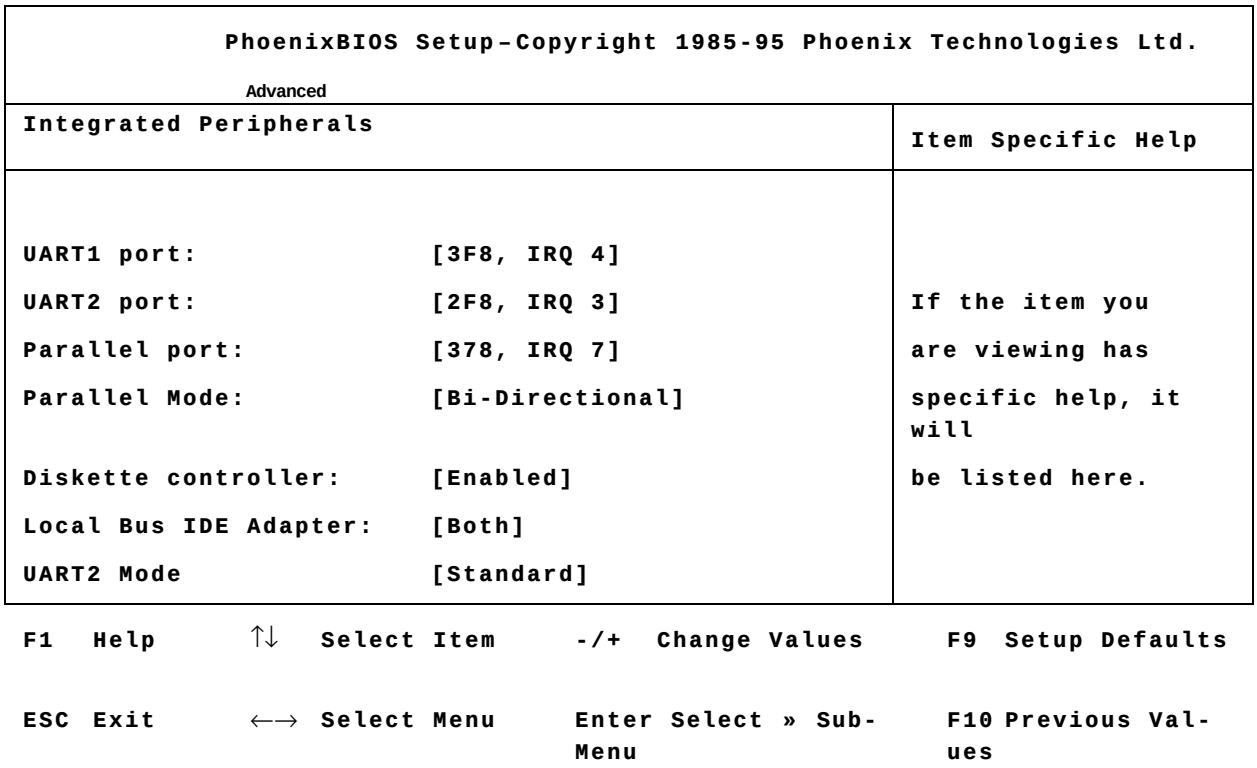

Figure Chapter 3 -8. Integrated Peripherals Sub-menu

Table Chapter 3 -8. Integrated Peripherals Sub-menu Options

Option	Description
UART1 Port	Allows the COM port address and IRQ levels to be modified or disabled.
UART2 Port	Allows the COM port address and IRQ levels to be modified or disabled.
Parallel Port	Select a unique address and interrupt request for the LPT port, or disable it. "Auto" selects the next available combination.
Parallel Mode	LPT port can be configured for bi-directional or output only.
Diskette Controller	Enables or disables the on-board floppy disk controller.
Local Bus IDE Adapter	Sets the local bus IDE adapter to Primary, Secondary, Both, or disables it..
UART2 Mode	Sets the interface to Standard or Infrared. Options are: Standard IrDA ASKIR

Advanced Chipset Control Sub-menu

Use this menu to change the values in the chipset registers and optimize your system's performance.

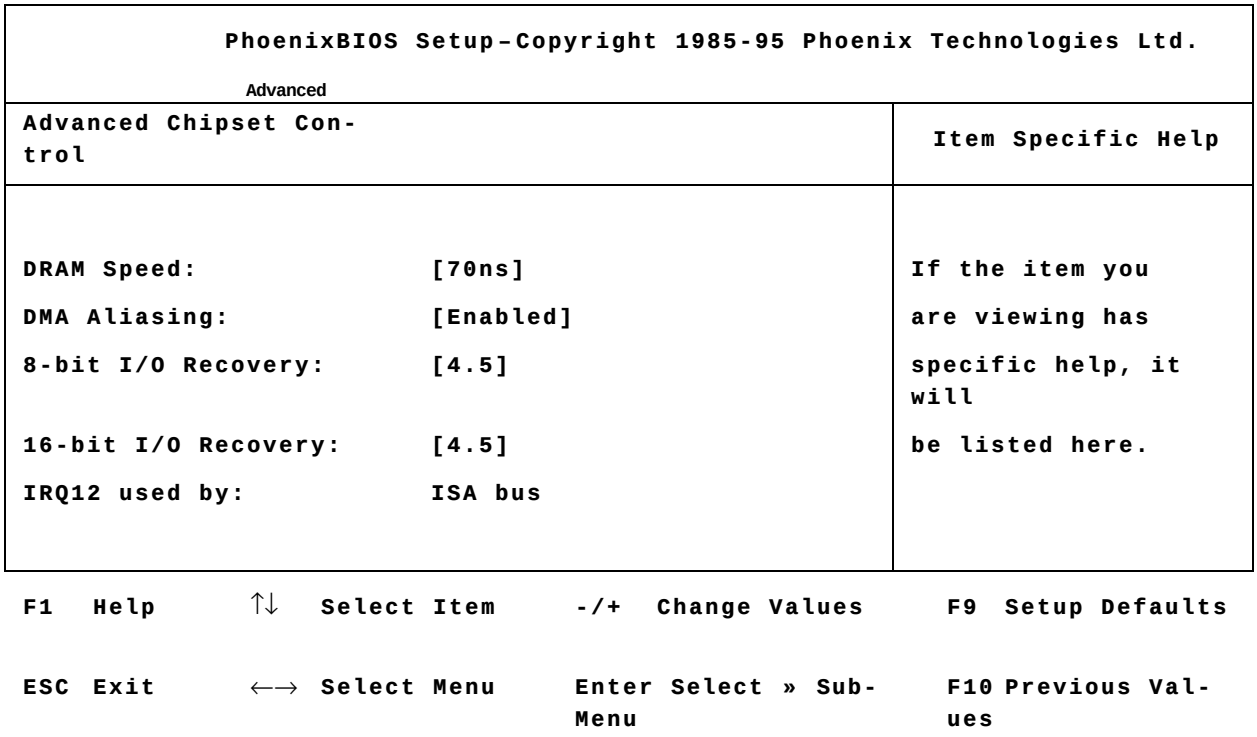

Figure Chapter 3 -9. Advanced Chipset Control Sub-menu

Table Chapter 3 -9 describes the available options on the Advanced Chipset Control Sub-menu.

Table Chapter 3 -9. Advanced Chipset Control Sub-menu Options

Option	Description
DRAM Speed	Speed of the SIMMs installed. This is used to configure the system for maximum performance.
DMA Aliasing	Disable DMA Aliasing if a device exists on the ISA bus that uses I/O ports 90h, 94h-96h, 98h, or 9Ch-9Eh.
8-bit I/O Recovery	Number of ISA clock cycles inserted between back-to-back I/O operations
16-bit I/O Recovery	Number of ISA clock cycles inserted between back-to-back I/O operations

Technical Note

Leave the options in this menu in their default configurations.

Security Menu

This menu prompts you for the new system password and requires you to verify the password by entering it again.

The password can be used to stop access to the setup menus or prevent unauthorized booting of the unit. The supervisor password can also be used to change the user password.

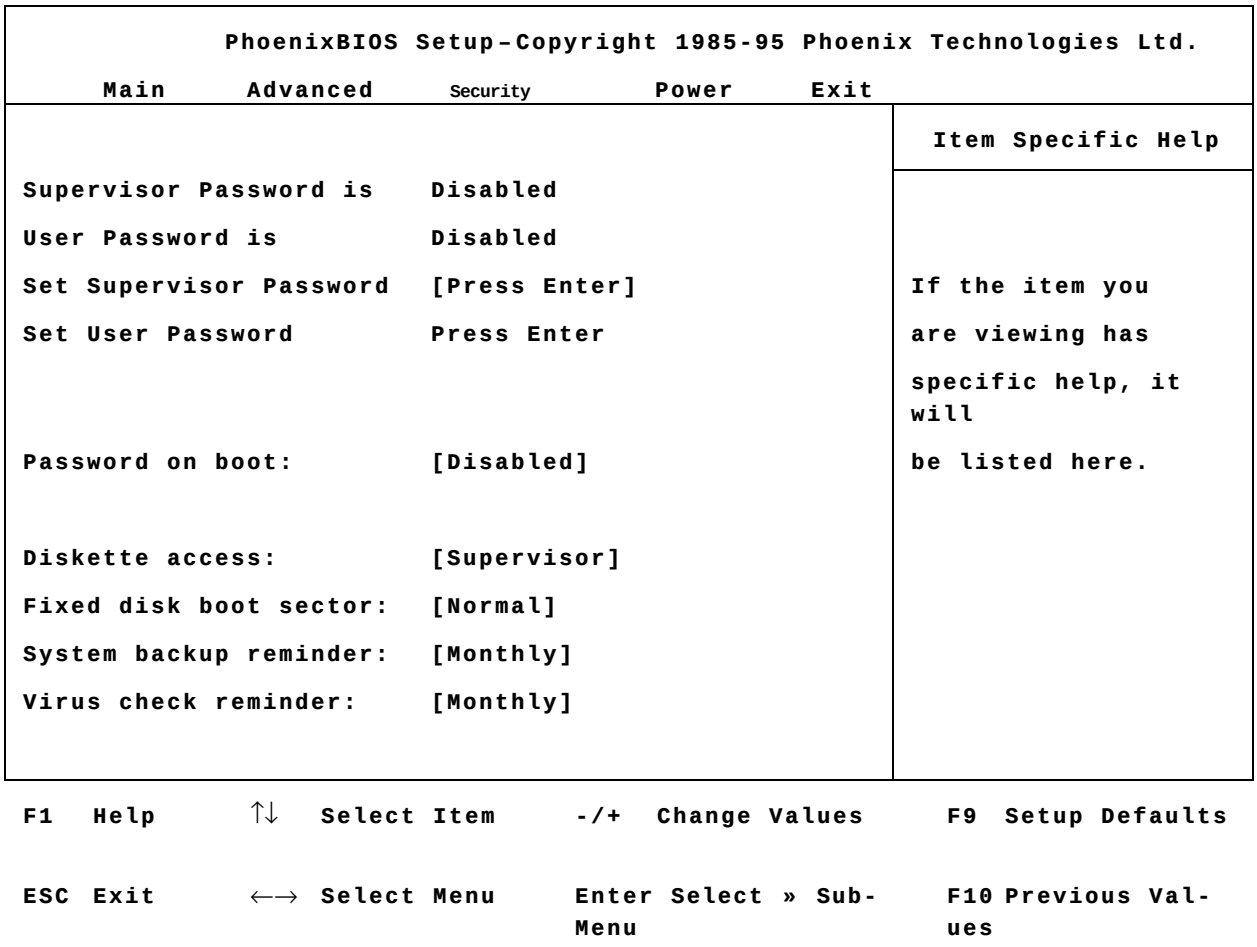

Figure Chapter 3 -10. Security Menu

Table Chapter 3 -10 describes the Security Menu options.

Table Chapter 3 -10. Security Menu Options

Option	Description
Supervisor Password	Provides full access to Setup menus. You may use up to seven alphanumeric characters. This option is disabled by setting it to [CR] or nothing.
Set User Password	Provides restricted access to Setup menus. It requires the prior setting of Supervisor password. You may use up to seven alphanumeric characters.
Password on Boot	If the supervisor password is set and this option is disabled, BIOS assumes the user is booting.
Diskette Access	Restricts access to floppy drives to the supervisor when set to “Supervisor.” Requires setting the Supervisor password.
Fixed Disk Boot Sector	Write protects the disk boot sector to help prevent viruses.
System Backup Reminder/Virus Check Reminder	Displays a message during boot up asking (Y/N) if you have backed-up the system or scanned it for any viruses. The message returns on each boot until you respond with "Y." It displays the message daily on the first boot of the day; weekly on the first boot after Sunday; and monthly on the first boot of the month.

Power Menu

```
            PhoenixBIOS Setup–Copyright 1985-95 Phoenix Technologies Ltd.
     Main     Advanced     Security     Power      Exit
                                                              Item Specific Help
APM:                        [Disabled]
Power Savings:              [Disabled]                        If the item you
                                                              are viewing has
Standby Timeout:            Disabled                          specific help, it
Suspend Timeout:            Disabled                          will
                                                              be listed here.
Standby CPU Speed:          MAX
Fixed Disk Timeout:         Disabled
CRT                         On

Standby Timer Reset
Events
Keyboard:                   [Enabled]
Mouse:                      [COM1(IRQ4)]

Standby Break Events
IRQ0:                       [Disabled]
IRQ1:                       [Auto]
IRQ3:                       [Auto]
IRQ4:                       [Auto]
IRQ5 thru 11:               [Disabled]
IRQ12:                      [Auto]
IRQ13 thru 15:              [Disabled]

Standby Wakeup Events
Keyboard:                   [Enabled]
Mouse:                      [COM1 (IRQ4)]

F1  Help   ↑↓  Select Item    -/+  Change Values    F9  Setup Defaults
```

```
ESC Exit      ←→ Select Menu    Enter Select » Sub-Menu    F10 Previous Values
```

Figure Chapter 3 -11. Power Menu

Table Chapter 3 -11 describes the options on the Power Menu.

Table Chapter 3 -11. Power Menu Options

Option	Description
APM	Sets power management options with predefined values.
Power Savings	Enables or disables power management. Options include: disable, minimum, medium, maximum, and customize. The customize option may be used to individually set standby timeout, suspend timeout, standby CPU speed, fixed disk timeout, and CRT values.
Standby Timeout	Sets an inactivity period required to put your system in standby (partial power shutdown).
Suspend Timeout	Sets an inactivity period required after standby to suspend (maximum power shutdown).
Standby CPU Speed	Sets CPU speed during standby. Available options are maximum/high, medium, or low speeds.
Fixed Disk Timeout	Sets an inactivity period of fixed disk required by standby (motor off). Available options are 16, 10, 5, 4, 3, 2, and 1 minute.
CRT	Off turns the CRT off on standby.
Standby Timer Reset Events	Sets keyboard or mouse to reset standby timer.
Keyboard	If enabled, key press will bring CPU out of standby.
Mouse	If enabled, mouse activity will bring CPU out of standby.
Standby Break Events	Events that will break out of standby modes.
IRQ0-IRQ15	Turns on the CPU clock when the IRQ is enabled during standby, and returns the system to full speed for the duration of the IRQ.
Standby Wakeup Events	Sets keyboard or mouse to bring CPU out of standby mode.

Exit Menu

This menu prompts you to exit setup.

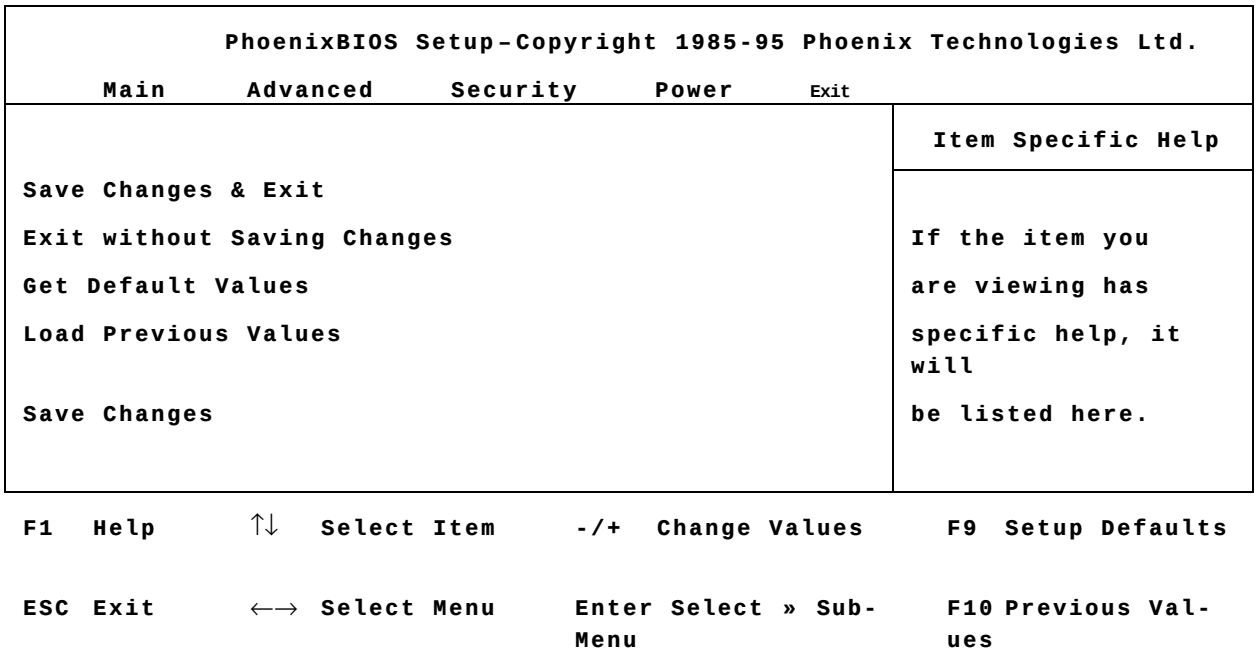

Figure Chapter 3 -12. Exit Menu

Table Chapter 3 -12 describes the Exit Menu options.

Table Chapter 3 -12. Exit Menu Options

Option	Description
Save Changes & Exit	After making your selections on the Setup menus, always select either “Save Changes & Exit" or "Save Changes." Both procedures store the selections displayed in the menus in battery-backed CMOS RAM. After you save your selections, the program displays this message: “Values have been saved.” “[Continue]” If you attempt to exit without saving, the program asks if you want to save before exiting. The next time you boot your computer, the BIOS configures your system according to the setup selections stored in CMOS. If those values cause the system boot to fail, reboot and press F2 to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.
Exit Without Saving Changes	Use this option to exit Setup without storing any new selections you may have made in CMOS. The selections previously in effect remain in effect.

Option	Description
Get Default Values	To display the default values for all the Setup menus, select this option. The program displays this message: **"Default values have been loaded."** **"[Continue]"** If during boot up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages: **"System CMOS checksum bad - run SETUP"** **"Press <F1> to resume, <F2> to Setup"** This means the CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Press F1 to resume the boot (this causes the system to be configured using the default values) or F2 to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.
Load Previous Values	If, during a Setup session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS. Selecting "Load Previous Values" updates all the selections and displays this message: **"Previous values have been loaded."** **"[Continue]"**
Save Changes	This option saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

BIOS Compatibility

This BIOS is IBM PC/AT compatible with additional CMOS RAM and BIOS data areas used.

Appendix A - DRAM Installation

The AHIP5+ has a two 72-pin in-line memory module (SIMM) site in which to add memory. Due to the CPU speed, SRAM access time should be 70 ns or less, and must be 60 ns to run with the fastest memory setting.

The AHIP5+ can accommodate 4, 8, 16, 32, or 64 Mbytes of SRAM. SIMM sizes of 1Mx32, 2Mx32, 4Mx32, 8Mx32, or 16Mx32 DRAM may be used.

Recommended manufacturers for DRAM, along with the respective part numbers, are listed below.

Table Appendix A -1. 1M x 32 Part Numbers (4 meg)

Manufacturer	Part Number	
	Non-EDO	EDO
Micron	MT8D132M-6	MT8D132M-6x
Reptron/PNY	N/A	ME10243208ES-60MT
Siemens	N/A	HYM3210055-60
Xycom	104273	

Table Appendix A -2. 2M x 32 Part Numbers (8 Meg)

Manufacturer	Part Number	
	Non-EDO	EDO
Hitachi	N/A	HB56U232SB-6C
Micron	MT6D232M-6	MT6D232M-6x
Reptron/PNY	N/A	ME20483216ES-60MT
Siemens	N/A	HYM322005S-60
Xycom	104258	

Table Appendix A -3. 4M x 32 Part Numbers (16 meg)

Manufacturer	Part Number	
	Non-EDO	EDO
Hitachi	N/A	HB56V832SB-6BN
Micron	MT8D432M-6	MT8D432M-6x
NEC	N/A	MC-42800F32B-60
Xycom	104302	

Table Appendix A -4. 8M x 32 Part Numbers (32 meg)

Manufacturer	Part Number (EDO)
Micron	MT16D832M-6x
Xycom	106054

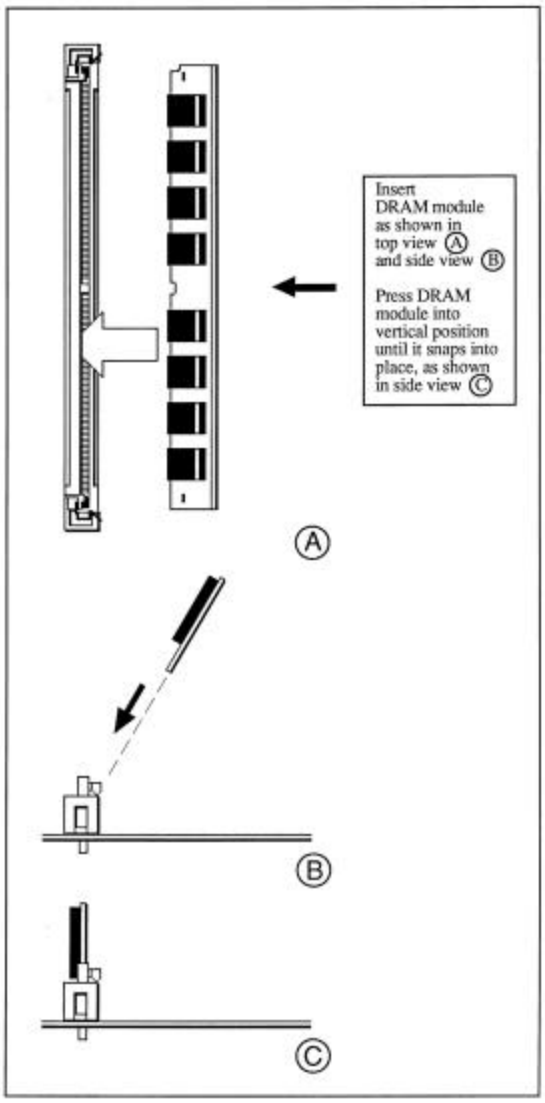

Figure A-1. DRAM Installation

Appendix B – Video Modes

Introduction

Appendix B defines the video modes and the panels the AHIP5+ supports.

Video Modes

The Chips & Technologies 65554 VGA controller supports many standard, VESA, and extended modes. The following tables list the standard and extended video modes and whether they passed, failed or are not supported with the CRT, TFT active color, or STN passive color displays.

Standard Modes

Mode IBM	VESA mode[1]	Number of colors	Pixels	Display mode	CRT	TFT	STN
00	-	16/256	320x200	text	OK	OK	OK
01	-	16/256	320x350	text	OK	OK	OK
02	-	16/256	640x200	text	OK	OK	OK
03	-	16/256	640x200	text	OK	OK	OK
04	-	4/256	320x200	graphics	OK	OK	OK
05	-	4/256	320x200	graphics	OK	OK	OK
06	-	2/256	640x200	graphics	OK	OK	OK
07	-	mono	720x350	text	OK	OK	OK
0D	-	16/256	320x200	graphics	OK	OK	OK
0E	-	16/256	640x200	graphics	OK	OK	OK
0F	-	mono	640x350	graphics	OK	OK	OK
10	-	16/256	640x350	graphics	OK	OK	OK
11,20	-	2/256	640x480	graphics	OK	OK	OK
12	-	16/256	640x480	graphics	OK	OK	OK
13	-	256/256	320x200	graphics	OK	OK	OK

- = Not supported by BIOS

[1] = Execute the VESA.EXE device driver to initiate VESA modes.

Extended Modes

Mode C&T	VESA mode[1]	Number of colors	Pixels	Display mode	CRT	TFT	STN
	100	256	640x400	graphics	OK	OK	OK
30	101	256	640x480	graphics	OK	OK	OK
40	unk	32K	640x480	graphics	OK	OK	OK
41	unk	64K	640x480	graphics	OK	OK	OK
50	unk	16M	640x480	graphics	OK	OK	OK
22	102	16	800x600	graphics	OK	-	-
32	103	256	800x600	graphics	OK	-	-
42	unk	32K	800x600	graphics	OK	-	-
43	unk	64K	800x600	graphics	OK	-	-
24	104	16	1024x768	graphics	OK	-	-
34	unk	256	1024x768	graphics	OK	-	-
44	unk	32K	1024x768	graphics	OK	-	-
45	unk	64K	1024,768	graphics	OK	-	-

- = Not supported by BIOS

[1] = Execute VESA.EXE device driver to initiate VESA modes.

Windows 3.1

Windows 3.1 driver (version 1.1.8)		CRT[3]	TFT	STN
C&T 65554	*1024x768x16*	YES	4	4
	1024x768x256	YES	4	4
	1024x768x32K	YES	4	4
	1024x768x64K	YES	4	4
	1280x1024x16	YES	4	4
	1280x1024x256	YES	4	4
	640x480x16	YES	YES	YES
	640x480x256	YES	YES	YES
	640x480x32k	YES	YES	YES
	640x480x64k	YES	YES	YES
	640x480x16M	YES	YES	YES
	800x600x16	YES	4	4
	800x600x256	YES	4	4
	800x600x32k	YES	4	4
	800x600x64k	YES	4	4
	800x600x16M	YES	4	4

[3] = All windows' drivers were tested on a NEC multisync 5FG monitor.
[4] = Scroll left or right to view entire screen.

Windows ‘95

Windows 95 driver (version 1.3.2 - included with Windows 95)	CRT[3]
C&T 65554 PCI 1024x768x16	YES
1024X768X256	YES
1024X768X16bit	YES
1024x768x24bit	YES
640x480x16	YES
640x480x256	YES
640x480x16bit	YES
640x480x24bit	YES
800x600x16	YES
800x600x256	YES
800x600x16bit	YES
800x600x24bit	YES

Appendix C – Pinouts

This appendix describes the pinouts for the AHIP5+ connectors defined in Chapter 2.

VGA Connector (VGA1)

The VGA connector is a 15 pin connector.

Pin	Signal
1	RED
2	GREEN
3	BLUE
4	NC
5	ORB_GND
6	ORB_GND
7	ORB_GND
8	ORB_GND
9	Fused VCC
10	ORB_GND
11	NC
12	DDCDAT
13	HSYNC
14	VSYNC
15	DDCCLK

NC = no connect

COM1 Connector RS-232/RS-485 (COM1_4)

The COM1 connector actually consists of 2 connectors attached to one logical port. Only one connector can be used at a time either the RS-485 port or the RS-232 port. The COM1 connector is a male DB-9 connector

Pin	Signal	Pin	Siganl
1A	DCD1	1B	TXD-
2A	RXD1	2B	TXD+
3A	TXD1	3B	TXD TERM -
4A	DTR1	4B	TXD TERM +
5A	GND	5B	GND
6A	DSR1	6B	RXD-
7A	RTS1	7B	RXD+
8A	CTS1	8B	RXD TERM +
9A	RI1	9B	RXD TERM -

Technical Note

'A' denotes the lower connector (RS-232) and 'B' denotes the upper connector (RS-485).

Technical Note

For TXD termination, connect a 150Ω, ½watt resistor from pin 3B to pin 4B, with pin 1B connected to pin 3B and pin 2B connected to pin 4B.

For RXD termination, connect a 150Ω, ½watt resistor from pin 8B to pin 9B, with pin 6B connected to pin 9B and pin 7B connected to pin 8B.

LPT1/COM2 RS-232 Connector (PARCOM2)

The COM2 connector is a male DB-25 connector. The COM2 port can be used for three separate devices but only one at a time:

- Touchscreen controller
- Infrared (IR) interface

- LPT1/COM2 RS-232 connector

The BIOS setup determines whether COM2 is used for the connector or the IR interface. Jumpers on the touchscreen controller board select the COM2 port or the AUX port. If COM2 is used for the touchscreen the COM2 mode must be set to standard.

'A' denotes the lower connector (LPT1) and 'B' denotes the upper connector (COM2, RS-232). This connector also contains the remote system reset option The reset jumper (J1) must be in position B for this option to work. The PB_RESET* pin must be switched to GND to reset the entire board.

Pin	Signal	Pin	Signal
1A	STROBE	1B	ORB_GND
2A	PD(0)	2B	TXD2
3A	PD(1)	3B	RXD2
4A	PD(2)	4B	RTS2
5A	PD(3)	5B	CTS2
6A	PD(4)	6B	DSR2
7A	PD(5)	7B	GND
8A	PD(6)	8B	DCD2
9A	PD(7)	9B	NC
10A	PACK	10B	NC
11A	PBUSY	11B	PB_RESET*
12A	PE	12B	NC
13A	SELECT	13B	NC
14A	AUTOFEED	14B	NC
15A	PERROR	15B	NC
16A	INIT	16B	NC
17A	SELIN	17B	NC
18A	GND	18B	NC
19A	GND	19B	NC
20A	GND	20B	DTR2
21A	GND	21B	NC
22A	GND	22B	RI2
23A	GND	23B	NC
24A	GND	24B	NC
25A	GND	25B	NC

FPGA Program Connector (J15)

This connector is used to program the lattice FPGA. This pinout matches the standard lattice pinout.

Pin	Signal
1	+5V
2	SDO*
3	SDI*
4	ISPEN*
5	NC
6	MODE*
7	GND
8	SCLK*

DCIN2 Power Connector (PWR2)

Together the DCIN1 and DCIN2 connectors accept a standard PS/2 style PC power supply connector.

Pin	Signal
1	NC
2	+5V
3	+12V
4	-12V
5	GND
6	GND

DCIN1 Power Connector (PWR1)

Pin	Signal
1	GND
2	GND
3	NC
4	+5V
5	+5V
6	+5V

Touch Control Connector (TCTRL1)

This connector provides the means to support 4-wire touchscreens, 5-wire touchscreens, and the method used on the 3200/3300 boards. This connector is latching to provide for a DRAM SIMM type installation.

This connector is used for the touchscreen controller.

Pin	Signal	Pin	Signal
1	+5V	21	GND
2	NC	22	KB_AIN0
3	+12V	23	GND
4	NC	24	KB_AIN1
5	NC	25	GND
6	-12V	26	RESET
7	NC	27	NC
8	NC	28	TXD2
9	+5V	29	NC
10	NC	30	TCH_RXD2
11	NC	31	NC
12	KB_P14	32	+5V
13	KB_P15	33	NC
14	KB_P16	34	AUX_DATA
15	KB_P17	35	AUX_CLK
16	NC	36	UL
17	NC	37	LL
18	GND	38	SENSE
19	TCH_LED*	39	LR
20	NC	40	UR

Touch Connector (TCH1)

This connector is the interface to the touch panel.

Pin	Signal
1	UR
2	LR
3	SENSE
4	LL
5	UL

Internal Mouse Connector (MS2)

This four-pin connector provides a future method to integrate a pointing device to the front panel.

Pin	Signal
1	GND
2	5VFUSE
3	AUX_CLK
4	AUX_DATA

Internal LED Connector (LEDMSC1)

This connector provides a method to add LED's to the touch only units. This connector also provides the pinout for the IR interface port.

Pin	Signal	Pin	Signal
1	5VFUSE	11	KSI(6)
2	NC	12	NC
3	5VFUSE	13	NC
4	NC	14	NC
5	GND	15	GND
6	IR_RXD2	16	COM_LED
7	TXD2	17	ALPHA_LED
8	IR_MODE	18	USER_LED
9	KSO(12)	19	IDEACTP_LED
10	KSI(7)	20	GND

LED In_Keypad Connector (LEDKB1)

This connector may be used for future designs which support the LEDs in the keypad.

Pin	Signal	Pin	Signal
1	IDEACTP_LED	6	GND
2	USER_LED	7	NC
3	ALPHA_LED	8	IR_MODE
4	COM_LED	9	TXD2
5	+5V (thru 330Ω res)	10	IR_RXD2

Flat Panel Connector (FPNL1)

The flat panel connector is a 60-pin SMD through board connector. It provides all the signals from the 65554 VGA controller along with +5V, GND, RESET, +12V, +3.3V, 4 flat panel detect signals, PANEL Logic Voltage, Switched VCC, and temperature/contrast control signals. The system board will support +5V and 3.3V TFT panels with a custom flat cable. It will support STN panels with a 2.5" X 2.75" PCB which contains the DC/DC for the custom VEE voltage along with the contrast and power sequencing circuit. There are also provisions to support a temperature sensor for automatic contrast control. Both the contrast and the temperature sensor are controlled by the 81C51SL.

The 4 flat panel select lines will be used to define up to 16 unique panel types. The cable will pull these signals to GND for low and leave them floating for a high. If all signals are high (No cable attached) the 9460 will default to CRT.

Pin	Signal	Pin	Signal
1	GND	31	GND
2	SHFCLK	32	P(4)
3	GND	33	P(5)
4	LP	34	P(6)
5	FLM	35	P(7)
6	GND	36	GND
7	P(16)	37	M
8	P(17)	38	VCCSW
9	P(18)	39	VCCSW
10	P(19)	40	+5V
11	GND	41	+5V
12	P(20)	42	PANEL_LOGIC
13	P(21)	43	PANEL_LOGIC
14	P(22)	44	+3.3V_CPU
15	P(23)	45	+3.3V_CPU
16	GND	46	GND
17	P(8)	47	FPSEL(0)
18	P(9)	48	FPSEL(1)
19	P(10)	49	FPSEL(2)
20	P(11)	50	FPSEL(3)
21	GND	51	+12V
22	P(12)	52	NC(Note 1)
23	P(13)	53	ENAVEE
24	P(14)	54	POT_DQ

Pin	Signal	Pin	Signal
25	P(15)	55	POT_CLK
26	GND	56	POT_RST*
27	P(0)	57	TEMP_RST*
28	P(1)	58	ENAVDD
29	P(2)	59	ENABCK
30	P(3)	60	RESET*

Backlight Inverter Connector (DCINV1)

This connector provides power for the backlight inverter.

Pin	Signal
1	+12V (switched)
2	+12V (switched)
3	Undefined Voltage
4	ENABKL (thru 10K Ω res
5	Undefined Voltage
6	Undefined Voltage
7	GND
8	GND

Internal Keyboard Connector (KYBD1)

Pin	Signal
1	KB_CLK
2	GND
3	KB_DATA
4	5VFUSE
5	SPEAKER

PS/2 Keyboard/AUX Connector (KBMS1)

This double stacked DIN connector provides an upper and lower connector for the keyboard and AUX port. Note: If the touchscreen controller is using the AUX port, this interface will not be available.

Pin	Signal	Pin	Signal
1A	KB_DATA	1B	AUX_DATA
2A	NC	2B	NC
3A	GND	3B	GND
4A	5VFUSE	4B	5VFUSE
5A	KB_CLK	5B	AUX_CLK
6A	NC	6B	NC

Internal Floppy Connector (FDD1)

Pin	Signal	Pin	Signal
1	+5V	14	FSTEP*
2	IDX*	15	GND
3	+5V	16	FWD*
4	FDS1*	17	GND
5	+5V	18	FWE*
6	DCHG*	19	GND
7	NC	20	FTK0*
8	NC	21	GND
9	NC	22	FWP*
10	MO1*	23	GND
11	NC	24	FRDD*
12	FDIRC*	25	GND
13	NC	26	FHS*

External Floppy Connector (FDD2)

Pin	Signal	Pin	Signal
1	+5V	14	FSTEP*
2	IDX*	15	NC
3	FDS1*	16	FWD*
4	+5V	17	GND
5	NC	18	FWE*
6	DCHG*	19	GND
7	NC	20	FTK0*
8	NC	21	GND
9	GND	22	FWP*
10	MO1*	23	GND
11	NC	24	FRDD*
12	FDIRC*	25	GND
13	NC	26	FHS*

IDE Connector (HDD1)

IDE hard drive connector HDD1 is a 40-pin header.

Pin	Signal	Pin	Signal
1	IDERESET*	21	HDRQ0
2	GND	22	GND
3	HDD7	23	HDIOW*
4	HDD8	24	GND
5	HDD6	25	HDIOR*
6	HDD9	26	GND
7	HDD5	27	HDIORDY
8	HDD10	28	ALE (pullup)
9	HDD4	29	HDAK0
10	HDD11	30	GND
11	HDD3	31	IRQ14
12	HDD12	32	HDIOCS16*
13	HDD2	33	HDA1
14	HDD13	34	NC
15	HDD1	35	HDA0
16	HDD14	36	HDA2
17	HDD0	37	HDCS0*
18	HDD15	38	HDCS1*
19	GND	39	IDEACTP*
20	NC	40	GND

ISA/IDE Backplane Connector (ATIDE1)

Pin	Signal	Pin	Signal
1	SD(7)	61	IOCHK*
2	SD(6)	62	RESETDRV
3	SD(5)	63	IRQ9
4	SD(4)	64	-5V (nc)
5	SD(3)	65	DRQ2
6	SD(2)	66	0WS*
7	SD(1)	67	IOCHRDY
8	SD(0)	68	AEN
9	SA(19)	69	SMEMW*
10	SA(18)	70	SMEMR*
11	SA(17)	71	IOW*
12	SA(16)	72	IOR*
13	SA(15)	73	DACK3*
14	SA(14)	74	DRQ3
15	SA(13)	75	DACK1*
16	SA(12)	76	DRQ1
17	SA(11)	77	REF*
18	SA(10)	78	SYSCLK
19	SA(9)	79	IRQ7
20	SA(8)	80	IRQ6
21	SA(7)	81	IRQ5
22	SA(6)	82	IRQ4
23	SA(5)	83	IRQ3
24	SA(4)	84	DACK2*
25	SA(3)	85	T/C
26	SA(2)	86	BALE
27	SA(1)	87	OSC
28	SA(0)	88	SBHE*
29	LA(23)	89	MEMCS16*
30	LA(22)	90	IOCS16*
31	LA(21)	91	IRQ10
32	LA(20)	92	IRQ11

Pin	Signal	Pin	Signal
33	LA(19)	93	IRQ12
34	LA(18)	94	IRQ15
35	LA(17)	95	IRQ14
36	SD(8)	96	DACK0*
37	SD(9)	97	MEMR*
38	SD(10)	98	DRQ0
39	SD(11)	99	MEMW*
40	SD(12)	100	DACK5*
41	SD(13)	101	DRQ5
42	SD(14)	102	DACK6*
43	SD(15)	103	DRQ6
44	HDDACK0*	104	DACK7*
45	HDDRQ0	105	DRQ7
46	RESERVED	106	MASTER16*
47	HDD(7)	107	IDERST*
48	HDD(6)	108	HDD(8)
49	HDD(5)	109	HDD(9)
50	HDD(4)	110	HDD(10)
51	HDD(3)	111	HDD(11)
52	HDD(2)	112	HDD(12)
53	HDD(1)	113	HDD(13)
54	HDD(0)	114	HDD(14)
55	HDIOW*	115	HDD(15)
56	HDIORDY	116	HDIOR*
57	IDE_IRQ	117	HDIOCS16*
58	HDA0	118	HDA1
59	HDCS0*	119	HDA2
60	IDEACTP*	120	HDCS1*

PCI Backplane Connector (PCIMG1)

Pin	Signal	Pin	Signal
1	+5V	61	-12V
2	+12V	62	GND
3	+5V	63	GND
4	+5V	64	NC
5	+5V	65	+5V
6	PIRQA*	66	+5V
7	PIRQC*	67	PIRQB*
8	+5V	68	PIRQD*
9	PCLKS3	69	REQ3*
10	+5V	70	REQ1*
11	NC	71	GNT3*
12	GND	72	GND
13	GND	73	GND
14	GNT1*	74	PCLKS2
15	PCIRST*	75	GND
16	+5V	76	PCLKS0
17	GNT0*	77	GND
18	GND	78	REQ0*
19	REQ2*	79	+5V
20	AD(30)	80	PAD(31)
21	+3.3V_CPU	81	PAD(29)
22	PAD(28)	82	GND
23	PAD(26)	83	PAD(27)
24	GND	84	PAD(25)
25	PAD(24)	85	+3.3V_CPU
26	GNT2*	86	C_BE*(3)
27	+3.3V_CPU	87	PAD(23)
28	PAD(22)	88	GMD
29	PAD(20)	89	PAD(21)
30	GND	90	PAD(19)
31	PAD(18)	91	+3.3V_CPU
32	PAD(16)	92	PAD(17)

Pin	Signal	Pin	Signal
33	+3.3V_CPU	93	C_BE*(2)
34	FRAME*	94	GND
35	GND	95	IRDY*
36	TRDY*	96	+3.3V_CPU
37	GND	97	DEVSEL*
38	STOP*	98	GND
39	+3.3V_CPU	99	PLOCK*
40	SDONE (pullup)	100	PERR*
41	SB0* (pullup)	101	+3.3V_CPU
42	GND	102	SERR*
43	PAR	103	+3.3V_CPU
44	PAD(15)	104	C_BE*(1)
45	+3.3V_CPU	105	PAD(14)
46	PAD(13)	106	GND
47	PAD(11)	107	PAD(12)
48	GND	108	PAD(10)
49	PAD(9)	109	GND
50	C_BE*(0)	110	PAD(8)
51	+3.3V_CPU	111	PAD(7)
52	PAD(6)	112	+3.3V_CPU
53	PAD(4)	113	PAD(5)
54	GND	114	PAD(3)
55	PAD(2)	115	GND
56	PAD(0)	116	PAD(1)
57	+5V	117	+5V
58	REQ64* (pullup)	118	ACK64* (pullup)
59	+5V	119	+5V
60	+5V	120	+5V

Keypad connector (KEYPAD1)

This connector is a 20-pin connector.

Pin	Signal	Pin	Signal
1	GND	11	KSI(7)
2	KSO(9)	12	KSO(0)
3	KSO(10)	13	KSO(1)
4	KSI(0)	14	KSO(2)
5	KSI(1)	15	KSO(3)
6	KSI(2)	16	KSO(4)
7	KSI(3)	17	KSO(5)
8	KSI(4)	18	KSO(6)
9	KSI(5)	19	KSO(7)
10	KSI(6)	20	KSO(8)