

CHIP4e+

Compact High-Integration
5x86 Platform with
Ethernet

P/N 128767-001A

<i>Revision</i>	<i>Description</i>	<i>Date</i>
A	Manual Released	3/98
B	Touchscreen Updates	7/02

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Chapter 1 – Module Overview

The Xycom Compact High-Integration 5x86™ Platform with Ethernet (CHIP4e+) is designed for use in Xycom's line of flat-panel industrial personal computers. The CHIP4e+ is optimized in design, layout, and features for use with these flat-panel computer systems. This integrated design approach allows Xycom industrial PC/ATs to incorporate "Big PC" features in an extremely compact package. These "Big PC" features include a 133 MHz CPU, PCI-bus SVGA controller, PCI IDE controller, PCI 10BASE-T/100BASE-TX controller, infrared port, and integrated touch screen.

Module Features

The CHIP4e+ offers the following features:

- 133 MHz Am5x86 CPU
- 4 to 64 Mbytes EDO DRAM
- PCI local bus SVGA controller
 - Jumper-selectable flat-panel interface that supports STN and TFT formats up to 640x480x16M
 - CRT interface that supports formats up to 1024x768x256
 - 1Mbyte video memory
- PCI fast IDE controller
- Two 16550-compatible serial ports
 - UART1: RS-232 or RS-485
 - UART2: RS-232 port, Infrared (IR), or touch screen
- Centronics-compatible parallel port
- PCI 10BASE-T/100BASE-TX Ethernet controller
- PC/104 support
- Floppy controller and external floppy connector
- PS/2 mouse and keyboard ports
- Real-time clock and battery
- Touch screen, keypad, and LED interfaces
- DOC2000 or 32Kx8 and 128Kx8 non-volatile SRAM support

Architecture

This section describes the architecture of the CHIP4e+ processor module.

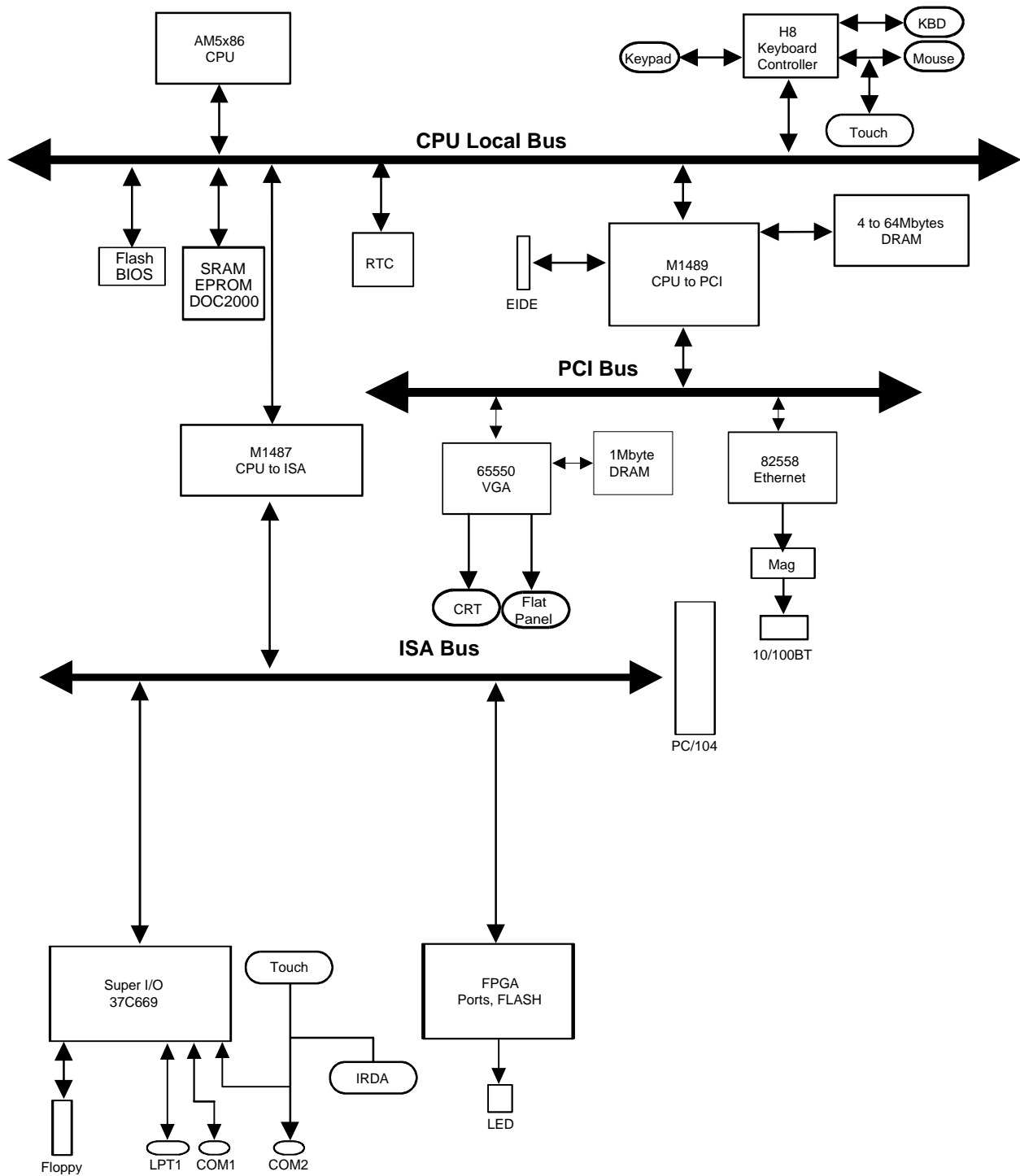


Figure 0-1. CHIP4e+ Functional Block Diagram

CPU

The CHIP4e+ incorporates an AMD® 5x86 processor with a CPU clock that runs quadrupled at 133 MHz with a 33 MHz external bus. The unified 16 Kbyte write-back cache technology minimizes the time the CPU core spends waiting for data or instructions, accelerating business and multimedia applications.

PCI Bus Interface

The FinALI chipset integrates a high-performance CPU-to-PCI interface capable of accelerated data transfers. The interface allows 32-bit master and slave PCI devices.

SVGA Graphics Controller

The PCI bus SVGA graphics controller supports CRTs and flat-panel displays with 1 Mbyte video DRAM. It supports resolutions of 640x480 with 16M colors; 800x600 with 64K colors; and 1024x768 with 256 colors.

Fast IDE controller

The high-speed local bus IDE controller supports programmed I/O (PIO) modes 0-4. It also provides 4x32-bit read-ahead buffer and 4x32-bit write-post buffer support to enhance IDE performance.

Caution

The IDE controller supports enhanced PIO modes, which reduce the cycle times for 16-bit data transfers to the hard drive. Check with your drive manual to see if the drive you are using supports these modes. The higher the PIO mode, the shorter the cycle time. As the IDE cable length increases, this reduced cycle time can lead to erratic operation. As a result, it is in your best interest to keep the IDE cable as short as possible.

Select the PIO modes in the BIOS setup (refer to Chapter 3). The autoconfigure classifies the drive connected if the drive supports the auto ID command. If you experience problems, change the PIO to standard.

Ethernet Controller

The CHIP4e+ contains a state-of-the-art 10BASE-T/100BASE-TX Ethernet controller with a 32-bit PCI bus-mastering interface to support 100-Mbits per second bus transfers. The controller serves as both a PCI master and slave. The Ethernet connector (ETHER1) provides auto-sensing for 10BASE-T and 100BASE-TX connections.

On-board Memory

DRAM

The CHIP4e+ has one 72-pin SIMM memory site, providing up to 64 Mbytes of DRAM. Populate the memory site with standard fast page mode memory or extended data out memory (EDO). EDO memory improves DRAM read performance.

Flash BIOS

The CHIP4e+ board provides a Flash BIOS location for system and video ROM. Table 0-1 describes the Flash memory map.

Table 0-1. Flash Memory Map

Device Address	Software	System Address
60000-7FFFFh	System BIOS	E0000-FFFFFh (also FFFE0000-FFFFFFFFh)
10000-5FFFFh	Undefined	
00000-0FFFFh	Video BIOS	C0000-CFFFFh

Non-Volatile SRAM or DOC2000 (optional)

Socket U25 is a 32-pin ROM site that provides an option for installing non-volatile SRAM or DiskonChip 2000 modules. You must specify which option you are installing on the BIOS Setup Advanced menu (refer to Chapter 3 for more information on the BIOS Setup menus).

Note

You may only install SRAM or DOC2000 in socket U25; you cannot install both.

Non-volatile SRAM contains a built-in battery and battery backup circuitry. Battery life is approximately seven years in the absence of VCC. Socket U25 supports 32Kx8 and 128Kx8 memory sizes. BIOS defines the location of SRAM as CC000.

DiskOnChip 2000 (DOC2000) is a Flash memory module. It contains an expansion BIOS that allows Flash memory to emulate a disk drive when the corresponding option is enabled in the BIOS Setup Advanced menu. If the system already incorporates a C: drive (IDE), DOC2000 becomes the D: drive. When installed, the DOC2000 module occupies memory address CC000-CFFFFh.

Serial and Parallel Ports

PC/AT peripherals include two high-speed, RS-232C, 16550-compatible serial ports and one bi-directional Centronics-compatible parallel port.

UART1 (COM1) accepts an RS-232 or a RS-485 connection (you can only use one connection at a time). UART2 (COM2) can be used for one of the following three options:

- RS-232 out the 25-pin DB connector
- Touch screen controller interface
- Infrared (IR) interface

Use the BIOS setup menus to configure the port as a serial or infrared port. You can use this port as both a serial and IR interface by allowing software to control the connection.

Note

You cannot use UART2 as a serial and IR port at the same time.

If the touch screen controller is jumpered to use UART2 as a serial device, the 25-pin DB connector cannot be used to interface to a device. These lines are combined internally.

Note

The BIOS setup menus for UART2 must be set to standard operation to use the touch screen controller on UART2.

Keyboard Ports

The keyboard port is routed to two separate connectors. One is a PS/2 connector, allowing the keyboard to be routed out the side of the unit; the other connector allows the keyboard to be routed to the front of the unit.

A polyswitch protects the +5 V on the keyboard port. This device opens if the +5 V is shorted to GND. Once you remove the shorting condition, the polyswitch allows current flow to resume.

Note

You can only use one keyboard port at a time.

Mouse Port

The CHIP4e+ supports two mouse ports. The external mouse port is routed to the PS/2 mouse connector; the internal mouse port is routed to the touch screen controller. If touch screen drivers are loaded, the external mouse port is disabled. Both the external port and the touch screen controller may be plugged in at the same time. However, the driver loaded may impair the operation of one of the ports. If the Microtouch mouse drivers are loaded, the external mouse port will use these drivers.

Note

When using the Xycom touchscreen controller (PIN 140554), the CHIP4e+ will behave the same. If using a PS/2 mouse is desired, install the Touch-Base touch driver in serial mode. In serial mode, the controller will use a COM port and free the PS/2 mouse port. Please follow the installation instructions on the Xycom documentation.

A polyswitch protects the +5 V on the mouse port. This device opens if the +5 V is shorted to GND. Once you remove the shorting condition, the polyswitch allows current flow to resume.

IR Interface

The IR interface, which uses UART2, is a half-duplex serial port capable of 115 Kbaud transfer rates. It also supports two transfer formats: IrDA and ASKIR. You must load software to support communication between two devices.

Flat-panel Interfaces

The CHIP4e+ incorporates two flat-panel connectors. The STN connector interfaces directly to STN flat panels. It provides a substrate voltage (VEE) of 34 volts, contrast control, and frame rate modulation to allow 4096 colors to be displayed. The TFT connector interfaces directly to TFT flat panels.

The flat-panel type is jumper selectable. Refer to Chapter 2 for jumper settings.

Floppy and Hard Drives

The CHIP4e+ can interface to a floppy drive via the external floppy connector. To connect a floppy drive to the external connector after power up, you must specify the floppy drive as a 1.44 Mbyte drive, and disable the floppy check option in the BIOS setup menus. If this is not done, the system will generate a floppy drive error during the Power On Self Test (POST).

The PCI-to-IDE interface supports one hard drive via the on-board IDE controller.

Caution

The total IDE cable length must not exceed 18 inches.

Keypad Interface

The CHIP4e+ provides a keypad interface. A connector supports up to a 10x8 scan matrix, which is combined with the keyboard bit stream by the keyboard controller.

Expansion Options

The CHIP4e+ provides a location to stack up to two PC/104 cards (refer to the *PC/104 Connector* section in Chapter 2).

Environmental Specifications

Table 0-2. Environmental Specifications

Characteristic	Specification
Temperature	
Operating	0° to 55° C (32° to 131° F)
Non-operating	-20° to 60°C (-4° to 140°F)
Humidity	
Operating	20% to 80% RH non-condensing
Non-operating	20% to 80% RH non-condensing
Altitude	
Operating	Sea level to 10,000 feet (3048 m)
Non-operating	Sea level to 40,000 feet (12192 m)
Vibration	
Frequency	5 to 2000 Hz
Operating	0.006" peak-to-peak displacement 1.0g maximum acceleration
Non-operating	0.015" peak-to-peak displacement 2.5 g maximum acceleration
Shock	
Operating	15g peak acceleration, 11 msec duration
Non-operating	30g peak acceleration, 11 msec duration

Hardware Specifications

Table 0-3. Hardware Specifications

Characteristic	Specification
Power Specifications	Typical Maximum
+12V	25ma 50ma
-12V	25ma 50ma
+5V	2.50 A 3.0A
CPU speed	133 MHz
PCI Super VGA Graphics Controller	1 Mbyte video DRAM STN and TFT support 640x480 16M colors 800x600 64K colors 1024x768 256 colors
Serial Ports (2)	16550 compatible UART1: RS-232 or RS-485 UART2: RS-232, IR, or touch-screen
Parallel Interface	Centronics compatible
On-board memory	4 to 64 Mbytes EDO DRAM
PCI Ethernet interface	10BASE-T/100BASE-TX
PCI IDE	Primary connector
Floppy drive	1.44 Mbyte (external option)
Expansion Options	PC/104 (-5 V is not supported)

Chapter 2 – Installation

This chapter provides information on configuring the CHIP4e+ processor module.

Figure 0-1 illustrates jumper and connector locations on the CHIP4e+.

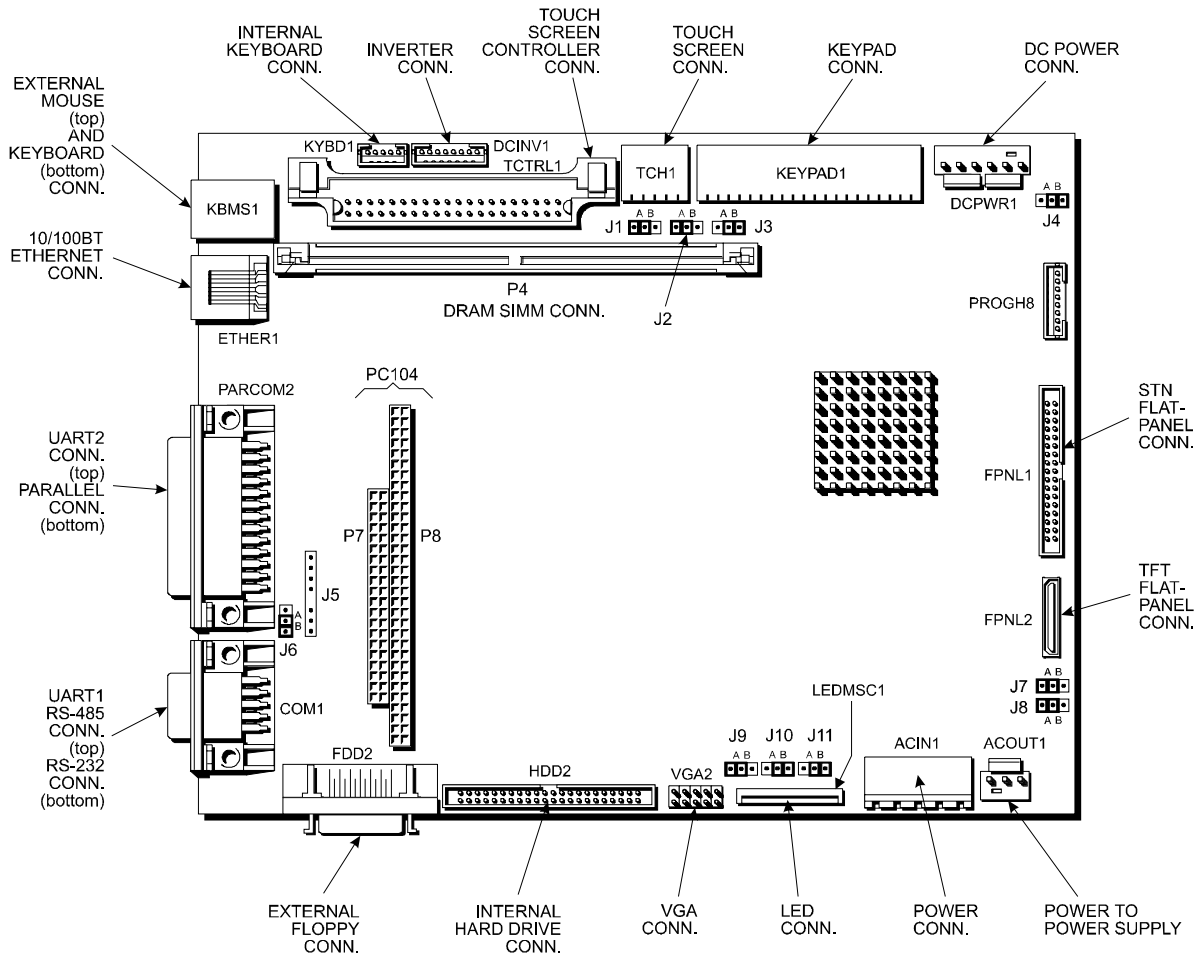


Figure 0-1. CHIP4e+ Jumper and Connector Locations

Configuration Options

Jumper Settings

Table 2-1 lists the module's jumpers, and their default positions and functions. The jumpers marked *Access* are at the top of the board for easy customer access.

Table 0-1. CHIP4e+ Jumpers

Jumper	Position	Function
J1	A ✓ B	Push button reset switch disabled (Access) Push button reset switch enabled
J2	A ✓ B	CMOS OK (Access) Clear CMOS
J3*	A B	Auto Detect (Access) CRT selected
J4	A ✓ B	Normal Program keyboard controller
J6	A ✓ B	Boot Flash enabled EPROM boot enabled
J7*	A B	+5V panel logic +3.3V panel logic (see Table 2-2)
J8	A ✓ B	VGA enabled VGA disabled
J9-J11*	A B	Panel type select (see Table 0-2)

✓ Indicates the default settings.

*Flat panel/CRT setting will dictate default settings on J3, J7, and J9-J11.

Table 0-2. Jumper-Selectable Panel Type

Panel Type	J7	J9	J10	J11
Sharp TFT 421/344 640x480 +5V	A	B	B	B
Kyocera STN 640x480 +5V	A	A	B	B
Kyocera STN 1024x768 +5V	A	B	A	B
Sharp TFT 1024x768 +5V	A	A	A	B
Kyocera STN 800x600 +3.3V	B	B	B	A
Sharp TFT 800x600 +3.3V	B	A	B	A

System Interrupts

Table 0-3 describes the interrupts used on the CHIP4e+.

Table 0-3. System Interrupts

Interrupt	Function
IRQ0	System Timer
IRQ1	Keyboard
IRQ2	Cascade
IRQ3	Serial Port*
IRQ4	Serial Port*
IRQ5	Parallel Port*
IRQ6	Floppy Controller
IRQ7	Parallel Port*
IRQ8	Real-Time Clock
IRQ9	Unused
IRQ10	Serial Port*
IRQ11	Serial Port*
IRQ12	Mouse Port
IRQ13	Math Coprocessor
IRQ14	Fixed Disk
IRQ15	Unused

*BIOS setup controlled

The BIOS setup menu controls the serial and parallel port interrupts. You can map the two serial ports to any two of the following interrupts: 3, 4, 10, or 11. The defaults are interrupts 3 and 4. This leaves IRQ10 and IRQ11 unused. You can map the parallel port to IRQ5 or IRQ7.

DMA Mapping

Table 0-4. DMA Channels

DMA	Function
-----	----------

DMA	Function
DMA0	Unused (Could be used for EPP/ECP parallel port option)
DMA1	Unused
DMA2	Floppy Controller
DMA3	Unused (Could be used for EPP/ECP parallel port option)
DMA5	Unused
DMA6	Unused
DMA7	Unused

DMA channels 0-3 are 8-bit; 5-7 are 16-bit. When the ECP option is enabled one of the 8-bit DMA channels is used.

Memory Map

Table 0-5 shows the CHIP4e+ memory map. The I/O designation refers to memory viewed as part of the AT bus.

Table 0-5. Memory Map

Address Range (hex)	Size	Device
FFFE0000 - FFFFFFFF	128 Kbytes	System BIOS
F8000000 - FFFEFFFF	~128 Mbytes	Allocated to PCI bus by BIOS or operating system
80000000 - F7FFFFFF	15 x 128 Mbytes	128 Mbytes blocks of F8000000-FFFFFFF (shadowed 15 times)
08000000 - 7FFFFFFF	15 x 128 Mbytes	128 Mbytes blocks of 0-07FFFFFF (shadowed 15 times)
04000000 - 07FFFFFF	64 Mbytes	Allocated to PCI bus by BIOS or operating system
00100000 - end of DRAM		DRAM
000F0000 - 000FFFFF	64 Kbytes	System BIOS
000E0000 - 000EFFFF	64 Kbytes	System BIOS
000D0000 - 000DFFFF	64 Kbytes	AT bus I/O
000CC000 - 000CFFFF	16 Kbytes	DOC2000 or Battery-backed SRAM option
000C0000 - 000CBFFF	48 Kbytes	VGA BIOS
000A0000 - 000BFFFF	128 Kbytes	VGA DRAM memory
00000000 - 0009FFFF	640 Kbytes	DRAM

I/O Map

Table 0-6 depicts the CHIP4e+'s I/O map. It contains the IBM AT architecture I/O ports, as well as some additions.

Table 0-6. I/O Map

Hex Range	Device
000-01F	DMA controller 1, 8237A-5 equivalent
020-021	Interrupt controller 1, 8259 equivalent
022	M1489/M1487 configuration index register
023	M1489/M1487 configuration data register
025-02F	Interrupt controller 1, 8259 equivalent
040-05F	Timer, 8254-2 equivalent
060-06F	8742 equivalent (keyboard)
070-07F	Real time clock bit 7 NMI mask
080-091	DMA page register
092	Reset/ Fast Gate A20
93-9F	DMA page register
0A0-0BF	Interrupt controller 2, 8259 equivalent
0C0-0DF	DMA controller 2, 8237A-5 equivalent
0F0	N/A
0F1	N/A
0F2-0F3	N/A
0F4	IDE ID port
0F5-0F7	N/A
0F8	IDE Index port
0F9-0FB	N/A
0FC	IDE Data port
0FD-0FF	N/A
100	Available
102	C&T Global enable register
103-179	Available
180-181	SRAM control register (may be remapped based on I/O port 234h)
182-1EF	Available
1F0-1F7	IDE controller (ATdrive)
231	Xycom LED port
233	Xycom Flash control register
234	Xycom I/O port control register
278-27F	Parallel port 2
280-2F7	Available
2F8-2FF	Serial port 2
300-36F	Available
370-377	Alternate floppy disk controller
378-37F	Parallel port 1
380-3AF	Available
3B0-3BB	Mono mode video
3BC-3BF	Reserved for parallel port
3C0-3CF	VGA/EGA2
3D0-3DF	CHIPS flat panel and color mode registers
3E0-3EF	Available
3F0-3F7	Primary floppy disk controller
3F8-3FF	Serial port 1
CF8	PCI configuration address register
CFC	PCI configuration data register

Note

Serial and parallel port addresses are controlled in the BIOS setup menus. Changing the setting changes the I/O location.

Note

Serial and parallel port interrupts are available if software does not use the ports or does not use the interrupt.

Registers

The CHIP4e+ contains three ports: 231h, 233h, and 234h.

Register 231h – CPU LED Port

Register 231h controls the LEDs and signals shown in Table 0-7.

Table 0-7. Register 231h - CPU LED Port

Bit	LED/Signal	Result	R/W
0	Reserved	0	R
1	DOC2000 EN	0 = Disable 1 = Enable	R
2	Reserved	0	R
3	Reserved	0	R
4	Reserved	0	R
5	ENFLASHWR	1 = Enables Flash write <i>Note: This bit must be 1 to make Flash visible at D0000h when booting from AT bus.</i>	R/W
6	VGA_EN	1 = Enables on-board VGA	R
7	CLRCMS	1 = CMOS okay 0 = Clear CMOS	R

Register 233h – Flash BIOS Control

Register 233h controls the signals shown in Table 0-8.

Table 0-8. Register 233h - Flash BIOS Control Register

Bit	Signal	Result	R/W
0	FLA15	Flash address 15 - page control bit	R/W
1	FLA16	Flash address 16 - page control bit	R/W
2	FLA17	Flash address 17 - page control bit	R/W
3	FLA18	Flash address 18 - page control bit	R/W
4	FPSEL0	Flat panel select bit 0	R
5	FPSEL1	Flat panel select bit 1	R
6	FPSEL2	Flat panel select bit 2	R
7	FPSEL3	Flat panel select bit 3	R

Register 234h – I/O Port Location

Register 234h controls the I/O port location register shown in Table 0-9.

Table 0-9. Register 234h - I/O Port Location Register

Bit	Signal	Result	R/W
0	Reserved	0	R
1	Reserved	0	R
2	Reserved	0	R
3	Reserved	0	R
4	Reserved	0	R
5	Reserved	0	R
6	I/O port bit0	0	R/W
7	I/O port bit1	0	R/W

Offset Registers

The following registers are located starting at the I/O location defined by register 234h, bits 6 and 7.

Table 0-10. I/O Port Selection (Port Address)

I/O Port Selection	Port Address
00	180h
01	2E0h
10	3E0h
11	300h

Offset 0 Page Register for Programming (Port Address)

Offset 0 is a read-only register that checks the battery status.

Table 0-11. Offset 0 Page Register for Programming (Port Address)

Bit	Signal	Result	R/W
0	Battery status	0 = Battery good 1 = Battery failed	R
1-7	Reserved	0	R

Offset 1 Page Register for Programming (Port Address +1)

Offset 1 controls the SRAM paging bits.

Table 0-12. Offset 1 Page Register for Programming (Port Address +1)

Bit	Signal	Result	R/W
0	Control RAM15	ROM address 15 - page control bit	R/W
1	Control RAM16	ROM address 16 - page control bit	R/W
2	Control RAM17	ROM address 17 - page control bit	R/W
3	Reserved	0	R
4	Reserved	0	R
5	Reserved		R/W
6	Reserved	0	R
7	Reserved	0	R

Connectors

This section describes the CHIP4e+ connectors and their pinouts.

Parallel Port Connector (PARCOM2)

This stacked 25-pin DB connector supports ECP and EPP. The A following the pin number indicates the parallel port connector; B indicates COM2.

Pin	Signal	Pin	Signal
1A	STROBE	1B	ORB_GND
2A	PD(0)	2B	TXD2
3A	PD(1)	3B	RXD2
4A	PD(2)	4B	RTS2
5A	PD(3)	5B	CTS2
6A	PD(4)	6B	DSR2
7A	PD(5)	7B	GND
8A	PD(6)	8B	DCD2
9A	PD(7)	9B	NC
10A	PACK	10B	NC
11A	PBUSY	11B	PB_RESET*
12A	PE	12B	NC
13A	SELECT	13B	NC
14A	AUTOFEED	14B	NC
15A	PERROR	15B	NC
16A	INIT	16B	NC
17A	SELIN	17B	NC
18A	GND	18B	NC
19A	GND	19B	NC
20A	GND	20B	DTR2
21A	GND	21B	NC
22A	GND	22B	RI2
23A	GND	23B	NC
24A	GND	24B	NC
25A	GND	25B	NC

Serial Port Connectors

There are two serial ports supported by the CHIP4e+ board.

COM1 Connector (COM1)

The nine-pin COM1 connector consists of two connectors (RS-232 and RS-485) attached to one logical port. Only one connector can be used at a time.

The A after the pin number in the following table indicates the lower connector (RS-232); B indicates the upper connector (RS-485).

Pin	Signal	Pin	Signal
1A	DCD1	1B	TXD-
2A	RXD1	2B	TXD+
3A	TXD1	3B	TXD TERM -
4A	DTR1	4B	TXD TERM +
5A	GND	5B	GND
6A	DSR1	6B	RXD-
7A	RTS1	7B	RXD+
8A	CTS1	8B	RXD TERM +
9A	RI1	9B	RXD TERM -

Note

For TXD termination, a 150Ω, ½-watt resistor must be connected from pin 3B to pin 4B, with pin 1B connected to pin 3B and pin 2B connected to pin 4B.

For RXD termination, a 150Ω, ½-watt resistor must be connected from pin 8B to pin 9B with pin 6B connected to pin 9B and pin 7B connected to pin 8B.

COM2 Connector (PARCOM2)

This 25-pin DB connector sits on top of the parallel port. You can use it for three separate devices, but you can connect only one at a time: the touch screen controller, infrared (IR) interface, or RS-232 connector. The BIOS setup determines whether COM2 is used for the RS-232 connector or the IR interface. Jumpers on the touch screen controller select the COM2 or mouse ports. If a touch screen controller is jumpered for COM2, COM2 is unavailable.

In the table below, the B following the pin number indicates COM2, the upper RS-232 port.

Pin	Signal	Pin	Signal
1A	STROBE	1B	ORB_GND
2A	PD(0)	2B	TXD2
3A	PD(1)	3B	RXD2
4A	PD(2)	4B	RTS2
5A	PD(3)	5B	CTS2
6A	PD(4)	6B	DSR2
7A	PD(5)	7B	GND
8A	PD(6)	8B	DCD2
9A	PD(7)	9B	NC
10A	PACK	10B	NC
11A	PBUSY	11B	PB_RESET*
12A	PE	12B	NC
13A	SELECT	13B	NC
14A	AUTOFEED	14B	NC
15A	PERROR	15B	NC
16A	INIT	16B	NC
17A	SELIN	17B	NC
18A	GND	18B	NC
19A	GND	19B	NC
20A	GND	20B	DTR2
21A	GND	21B	NC
22A	GND	22B	RI2
23A	GND	23B	NC
24A	GND	24B	NC
25A	GND	25B	NC

This connector also contains the remote system reset option. A normally open push button switch can be connected to pins 11B and 7B. When the switch is pressed the PB_RESET* signal is forced to GND, which causes the CPU to reset. You must set jumper J1 to position B to enable this option.

PS/2 Keyboard and Mouse Port Connector (KBMS1)

This double-stacked connector provides an upper and lower connector for the keyboard and mouse port. The keyboard connector is the lower six-pin connector. This port uses a polyswitch to protect VCC from directly shorting to GND.

Pin	Signal	Pin	Signal
1A	KB_DATA	1B	AUX_DATA
2A	NC	2B	NC
3A	GND	3B	GND
4A	5VFUSE	4B	5VFUSE
5A	KB_CLK	5B	AUX_CLK
6A	NC	6B	NC

Internal Keyboard Connector (KYBD1)

KYBD1 is a five-pin internal keyboard connector.

Note

This connector and the external connector cannot be used at the same time.

Pin	Signal
1	KB_CLK
2	GND
3	KB_DATA
4	5VFUSE
5	SPEAKER

VGA Connector (VGA2)

VGA2 is a 10-pin dual-row header. This connector is enabled when J3 is set to B.

Pin	Signal
1	RED
2	GND
3	GREEN
4	GND
5	BLUE
6	GND
7	VSYNC
8	GND
9	HSYNC
10	GND

External Floppy Drive Connector (FDD2)

FDD2 is a 26-pin external floppy connector. This port uses a polyswitch to protect VCC from directly shorting to GND.

Pin	Signal	Pin	Signal
1	+5V_FUSED	14	FSTEP*
2	IDX*	15	NC
3	FDS1*	16	FWD*

4	+5V_FUSED	17	GND
5	NC	18	FWE*
6	DCHG*	19	GND
7	NC	20	FTK0*
8	NC	21	GND
9	GND	22	FWP*
10	MO1*	23	GND
11	NC	24	FRDD*
12	FDIRC*	25	GND
13	NC	26	FHS*

Internal LED Connector (LEDMSC1)

This 20-pin connector provides a way to add LEDs to touch screen units. This connector also serves as the IrDA interface port connector.

Pin	Signal	Pin	Signal
1	5VFUSE	11	UC_CONT
2	NC	12	NC
3	5VFUSE	13	NC
4	NC	14	NC
5	GND	15	GND
6	IR_RXD2	16	COM_LED
7	TXD2	17	ALPHA_LED
8	IR_MODE	18	USER_LED
9	GND	19	IDEACTP_LED
10	DC_CONT	20	GND

FPGA Program Connector (J5)

This eight-pin connector is used to program the lattice FPGA.

Pin	Signal
1	+5V
2	SDO*
3	SDI*
4	ISPEN*
5	NC
6	MODE*
7	GND
8	SCLK*

IDE Connector (HDD2)

HDD2 is a dual-row, 44-pin 2mm box header provides an interface to an IDE hard drive.

Pin	Signal	Pin	Signal
1	IDERESET*	23	HDIOW*
2	GND	24	GND
3	HDD7	25	HDIOR*
4	HDD8	26	GND
5	HDD6	27	HDIORDY
6	HDD9	28	ALE (pullup)
7	HDD5	29	NC
8	HDD10	30	GND
9	HDD4	31	IRQ14
10	HDD11	32	HDIOWS16*
11	HDD3	33	HDA1
12	HDD12	34	NC
13	HDD2	35	HDA0
14	HDD13	36	HDA2
15	HDD1	37	HDCS0*
16	HDD14	38	HDCS1*
17	HDD0	39	IDEACTP*
18	HDD15	40	GND
19	GND	41	+5V
20	NC	42	+5V
21	NC	43	GND
22	GND	44	NC

Power Connectors (DCPWR1)

DCPWR1 is a six-pin connector.

Pin	Signal
1	+12V
2	+5V
3	+5V
4	GND
5	GND
6	-12V

Touch Control Connector (TCTRL1)

TCTRL1 is a 40-pin latching connector providing touch screen control.

Pin	Signal	Pin	Signal
1	+5V	21	GND
2	NC	22	NC
3	+12V	23	GND
4	NC	24	NC
5	NC	25	GND
6	-12V	26	RESET
7	NC	27	NC
8	NC	28	TXD2
9	+5V	29	NC
10	NC	30	TCH_RXD2
11	NC	31	NC
12	NC	32	+5V
13	NC	33	NC
14	NC	34	AUX_DATA
15	NC	35	AUX_CLK
16	NC	36	UL
17	NC	37	LL
18	GND	38	SENSE
19	TCH_LED*	39	LR
20	NC	40	UR

Touch Connector (TCH1)

This five-pin connector interfaces to the touch screen.

Pin	Signal
1	UR
2	LR
3	SENSE
4	LL
5	UL

STN Flat-Panel Connector (FPNL1)

The 34-pin FPNL1 connects to a STN flat-panel display. The flat-panel type and panel logic voltage are jumper selectable (refer to the *Jumper Settings* section earlier in this chapter).

Pin	Signal	Pin	Signal
1	LP(15)	18	LP
2	LP(14)	19	GND
3	LP(13)	20	SHFCLK
4	LP(12)	21	GND
5	LP(7)	22	LP(11)
6	LP(6)	23	LP(10)
7	LP(5)	24	LP(9)
8	LP(4)	25	LP(8)
9	VCCSW	26	LP(3)
10	GND	27	LP(2)
11	NC	28	LP(1)
12	SW_VEE	29	LP(0)
13	SW_VEE	30	NC
14	VCONT	31	NC
15	FLM	32	+5V
16	NC	33	SWVCC
17	ENAVEE(DISP)	34	WIPER

TFT Flat-Panel Connector (FPNL2)

The 31-pin FPNL2 connects to a TFT flat-panel display. The flat-panel type and panel logic voltage are jumper selectable (refer to the *Jumper Settings* section earlier in this chapter).

Pin	Signal	Pin	Signal
1	GND	17	LP(14)
2	SHFCLK	18	LP(15)
3	LP	19	GND
4	FLM	20	LP(2)
5	GND	21	LP(3)
6	LP(18)	22	LP(4)
7	LP(19)	23	LP(5)
8	LP(20)	24	LP(6)
9	LP(21)	25	LP(7)
10	LP(22)	26	GND
11	LP(23)	27	M
12	GND	28	VCCSW
13	LP(10)	29	VCCSW
14	LP(11)	30	R/L
15	LP(12)	31	U/D
16	LP(13)		

Backlight Inverter Connector (DCINV1)

This eight-pin connector provides power for the backlight inverter.

Pin	Signal
1	+12V (switched)
2	+12V (switched)
3	Undefined Voltage
4	Undefined Voltage
5	Undefined Voltage
6	Undefined Voltage
7	GND
8	GND

Caution

Do not use excessive force or pressure to engage the connectors.

AC Input Connector (ACIN1)

Pin	AC Signal	DC Signal
1	L	+DC
2	N	-DC
3	AC_GND	GND

AC Supply Connector (ACOUT1)

This three-pin connector connects the power supply to the CPU.

Pin	AC Signal	DC Signal
1	L	+DC
2	NC	NC
3	N	-DC

H8 Boot Program (PROGH3)

This eight-pin connector programs the H8 for the first time.

Pin	Signal
1	GND
2	TXD1
3	RXD1
4	RES*
5	+5V
6	+12V
7	MD1
8	GND

Ethernet Connector (ETHER1)

This eight-pin connector provides 10BASE-T and 100BASE-TX Ethernet connections.

Pin	Signal
1	TX+
2	TX-
3	RX+
4	Short to pin 5 75ohm to TERMPANE
5	Short to pin 4 75ohm to TERMPANE
6	RX-
7	Short to pin 8 75ohm to TERMPANE
8	Short to pin 7 75ohm to TERMPANE

PC/104 Connector (P7 and P8)

This 32-pin connector allows you to connect PC/104 cards.

Note

The PC/104 connector does not support cards that need -5V.

Pin	Row A	Row B	Row C	Row D
-----	-------	-------	-------	-------

0	-	-	GND	GND
1	IOCHCK*	GND	SBHE*	MEMCS16*
2	SD7	RESETDRV	LA23	IOCS16*
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	NC	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	0WS*	LA17	DACK0*
9	SD0	+12V	MEMR*	DRQ0
10	IOCHRDY	NC	MEMW*	DACK5*
11	AEN	SMEMW*	SD8	DRQ5
12	SA19	SMEMR*	SD9	DACK6*
13	SA18	IOW*	SD10	DRQ6
14	SA17	IOR*	SD11	DACK7*
15	SA16	DACK3*	SD12	DRQ7
16	SA15	DRQ3	SD13	+5V
17	SA14	DACK1*	SD14	MASTER*
18	SA13	DRQ1	SD15	GND
19	SA12	REF*	NC	GND
20	SA11	SYSCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2*		
27	SA4	TC		
28	SA3	ALE		
29	SA2	+5V		
30	SA1	OSC		
31	SA0	GND		
32	GND	GND		

Keypad Connector (KEYPAD1)

This 20-pin connector provides the keypad interface.

Pin	Signal	Pin	Signal
1	GND	11	KSI(7)
2	KSO(9)	12	KSO(0)
3	KSO(10)	13	KSO(1)
4	KSI(0)	14	KSO(2)
5	KSI(1)	15	KSO(3)
6	KSI(2)	16	KSO(4)
7	KSI(3)	17	KSO(5)
8	KSI(4)	18	KSO(6)
9	KSI(5)	19	KSO(7)
10	KSI(6)	20	KSO(8)

Chapter 3 – BIOS Setup Menus

The CHIP4e+ board's customized BIOS has been designed to surpass the functionality provided for normal PC/ATs. This custom BIOS allows you to access the value-added features on the CHIP4e+ module without interfacing to the hardware directly.

Moving through the Menus

General instructions for navigating through the screens are described below:

Key	Result
F1 or ALT-H	Opens the General Help window
F2	Enters the BIOS setup menus
ESC	If you are in a submenu, it returns to its associated menu. If you are in a menu, it accesses the Exit menu.
← or → arrow keys	Selects a different menu
↓ or ↑	Moves the cursor to the next or previous user-configurable field in the menu
TAB	Moves the cursor to the next user-configurable field in the menu. When you reach the last user-configurable field in the menu, it cycles to the first user-configurable field in the menu.
SHIFT+TAB	Moves the cursor to the previous user-configurable field in the menu. When you reach the first user-configurable field in the menu, it cycles to the last user-configurable field in the menu.
HOME and PGUP or END and PGDN	Moves the cursor to the first or last user-configurable field in the menu
F5 or -	Selects the previous value for the field
F6 or + or SPACE	Selects the next value for the field
F9	Loads the menu's default configuration values
F10	Loads the menu's previous configuration values
ENTER	Executes the selected command or opens the selected submenu (a "▣" indicates a submenu)
ALT-R	Refresh screen

Note

The settings shown in the menus are the default settings.

BIOS Main Menu

Follow the instructions below to access the BIOS setup menus:

- If the setup prompt is disabled on your system—which is the default—press F2 as soon as the “Xycom Industrial BIOS vx.x” banner displays at the top of your screen, and before your system loads the operating system.
- If the setup prompt is enabled on your system (on the Boot Sequence submenu), the BIOS displays the following message: “Press F2 to enter Setup.” As soon as this message appears, press F2.

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.			
Main	Advanced	Security	Exit
System Time:	[16:19:20]		
System Date:	[02/25/1998]		
Diskette A:	[1.44 MB, 3½"]		
Diskette B:	[Not Installed]		
<input checked="" type="checkbox"/> IDE Adapter 0 Master	(C: 1350 Mb)		
<input checked="" type="checkbox"/> IDE Adapter 0 Slave	(None)		
Video System:	[EGA / VGA]		
<input checked="" type="checkbox"/> Memory Shadow			
<input checked="" type="checkbox"/> Boot sequence:	[A: then C:]		
<input checked="" type="checkbox"/> Numlock:	[Auto]		
System Memory:	640 KB		
Extended Memory:	3 MB		

Item Specific Help
If the line item you are viewing has specific help, it will be listed here.

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults

ESC Exit ←→ Select Menu Enter Select Submenu F10 Previous Values

Option	Description
System Time (HH/MM/SS)	Sets the real-time clock for hour, minute, and seconds. The hour is calculated according to a 24-hour military clock (i.e., 00:00:00 through 23:59:59). Use TAB to move right; SHIFT + TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to enter the seconds or type zeros in front of numbers.
System Date (MM/DD/YYYY)	Sets the real-time clock for the month, day, and year. Use TAB to move right; SHIFT + TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to type zeros in front of numbers.
Diskette A or B	Selects the floppy-disk drive installed in your system.
Video System	Selects the default video device.
System Memory	Displays the amount of conventional memory detected during boot up. This field is not user configurable.
Extended Memory	Displays the amount of extended memory detected during boot up. This field is not user configurable.

IDE Adapter 0 Master and Slave Submenu

Use the IDE Adapter 0 Master and Slave submenus to configure IDE hard drive information. If one drive is attached to the IDE adapter, then you need to enter Master Submenu parameters. If two drives are connected, you need to enter both Master and Slave Submenu parameters. The Master and Slave submenus contain the same information.

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.	
Main	
IDE Adapter 0 Master (C: 1350 Mb)	Item Specific Help
Autotype Fixed Disk: [Press Enter]	If the line item you are viewing has specific help, it will be listed here.
Type: [Auto]	
Cylinders:	
Heads:	
Sectors/Track:	
Write Precomp:	
Multi-Sector Transfers: Disabled	
LBA Mode Control: Disabled	
32 Bit I/O: [Disabled]	
Transfer Mode: Standard	

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults

ESC Exit ←→ Select Menu Enter Select ▣ Submenu F10 Previous Values

Option	Description
Autotype Fixed Disk	Reads the hard disk parameters from the drive if you press ENTER. Do not attempt to manually set the disk drive parameters unless instructed to do so by Xycom Application Engineering.
Type	Options include 1 to 39, User, or Auto. The "1 to 39" option fills in all remaining fields with values for predefined disk type. "User" prompts you to fill in remaining fields. "Auto" autotypes at each boot, displays settings in setup menus, and does not allow you to edit the remaining fields.
Cylinders	Indicates the number of cylinders on the hard drive. This information is automatically entered if the "Autotype Fixed Disk" option is set.
Heads	Indicates the number of read/write heads on the hard drive. This information is automatically entered if the "Autotype Fixed Disk" option is set.
Sectors/Track	Indicates the number of sectors per track on the hard drive. This information is automatically entered if the "Autotype Fixed Disk" option is set.
Write Precomp	This value is not used or required by IDE hard drives.
Multi-Sector Transfers	Sets the number of sectors per block. Options are Auto, 2, 4, 8, or 16 sectors. "Auto" sets the number of sectors per block to the highest number supported by the drive.
LBA Mode Control	Enables Logical Block Access. The default is enabled and should work with most hard drives.
32-Bit I/O	Enables 32-bit communication between the CPU and IDE interface.
Transfer Mode	Selects the method for transferring the data between the hard disk and system memory. Available options are determined by the drive type and cable length.

Memory Shadow Submenu

This screen displays the amount of shadow memory in use.

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.	
Main	
Memory Shadow	Item Specific Help
System shadow: Enabled Video shadow: [Enabled]	If the line item you are viewing has specific help, it will be listed here.

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
 ESC Exit ←→ Select Menu Enter Select ▣ Submenu F10 Previous Values

Option	Description
System Shadow	Shadow memory is used to copy system and/or video BIOS into RAM to improve performance. This field is not user configurable.
Video shadow	When enabled, video BIOS is copied to shadow RAM for increased performance. The CHIP4e+ is shipped with video BIOS shadowed.

Boot Sequence Submenu

Use this menu to configure the boot sequence.

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.		
Main		
Boot Sequence		Item Specific Help
Previous Boot:	[Disabled]	If the line item you are viewing has specific help, it will be listed here.
Boot sequence:	[A: then C:]	
SETUP prompt:	[Disabled]	
POST Errors:	[Enabled]	
Floppy check:	[Disabled]	
Summary screen:	[Enabled]	

F1 Help ↑↓ Select -/+ Change Values F9 Setup Defaults
 Item

ESC Exit ←→ Select Enter Select ▣ Submenu F10 Previous Values
 Menu

Option	Description
Previous Boot	Detects if a boot sequence was not completed properly when enabled. An incomplete boot may be caused by a power failure, reset during boot up, or invalid CMOS configuration. If the BIOS detects this condition, it will display the following message: "Previous boot incomplete - default configuration used." The system is then rebooted using the default configuration. If this option is disabled, the system BIOS will not detect an incomplete boot. As a result, the system may not boot if the CMOS settings are wrong.
Boot Sequence	Attempts to load the operating system from the disk drives in the sequence selected here.
Setup Prompt	Displays the message, "Press <F2> for Setup," during boot up.
POST Errors	Halts the system if it encounters a boot error when enabled, and will display "Press <F1> to resume, <F2> for Setup."
Floppy Check	Seeks disk drives on the system during boot up if enabled. Disabling speeds boot time.
Summary Screen	Displays system summary screen during boot up when enabled. The default is enabled. This screen is a standard Phoenix BIOS screen and provides information on the following items: Processor Type COM Ports Coprocessor Type LPT Ports BIOS Date Display Type System ROM Address Hard Disk 0 System RAM Hard Disk 1 Extended RAM Diskette A Shadow RAM Diskette B Cache RAM

Numlock Submenu

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.		
Main		
Keyboard Features		Item Specific Help
Numlock:	[Auto]	If the line item you are viewing has specific help, it will be listed here.
Key Click:	[Disabled]	
Keyboard auto-repeat rate:	[30/sec]	
Keyboard auto-repeat delay:	[1/2 sec]	

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults

ESC Exit ←→ Select Menu Enter Select ▣ Submenu F10 Previous Values

Option	Description
Numlock	Determines how the BIOS defines the numlock key at power up or soft reset. Normally, the BIOS sets the numlock (numeric keys selected) if it detects a 101- or 102-key keyboard at power up. If an 84-key keyboard is detected, numlock is turned off (cursor keys selected). Select "Auto" to keep this state; "On" to select the numeric keys, regardless of keyboard; or "Off" to select the cursor keys, regardless of keyboard.
Keyboard Click	Provides audible key-press feedback by causing the BIOS to click through the system speaker every time a key is pressed, if enabled. This option is only valid for systems with a speaker connected to the speaker jack.
Keyboard auto-repeat rate	Defines the rate at which the keyboard repeats while a key is pressed. The higher the number, the faster the key repeats.
Keyboard auto-repeat delay	Sets the delay time after a key is held down, before it begins to repeat the keystroke.

Advanced Menu

This menu lets you change peripheral control, advanced chipset control, and disk access mode.

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.	
Main	Advanced
Security Exit	
Warning!	
Setting items on this menu to incorrect values may cause your system to malfunction.	
<input type="checkbox"/> Integrated Peripherals <input type="checkbox"/> Advanced Chipset Control	
Plug & Play O/S:	[No]
Large Disk Access Mode:	[DOS]
Simultaneous Video:	[Disabled]
Video Screen Expansion:	[Video BIOS Default]
32-Pin ROM Site Type:	[SRAM]
Item Specific Help	
If the line item you are viewing has specific help, it will be listed here.	

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults

ESC Exit ←→ Select Menu Enter Select Submenu F10 Previous Values

Feature	Description
Plug & Play O/S	Select "Yes" if using an operating system with Plug & Play capabilities.
Large Disk Access Mode	Select "DOS" if your system has DOS. Select "Other" if you have another operating system, such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads, or more than 63 tracks per sector.
Simultaneous Video	Select "Enabled" if you want both a video display out the CRT port and the flat-panel display. Select "Disabled" if you want only the flat-panel display. <i>Note: If you enable this option, it will degrade passive STN panel performance.</i>
Video Screen Expansion	Enables video screen expansion to fill the area of the flat-panel screen. Used most for DOS, the setting for each option depends on the type of flat panel attached to the unit. "ON" maximizes expansion as allowed for the panel, while "OFF" minimizes expansion as allowed for the panel. For non-DOS operating systems, use "Video BIOS Default."
32-Pin ROM Site	Sets the type of device installed in the 32-Pin ROM site. Select "Disk-On-Chip" if the site is filled with a DiskOnChip 2000. Select "SRAM" if the site is unpopulated or filled with SRAM.

Integrated Peripherals Submenu

The Integrated Peripherals Submenu is used to configure the COM ports, parallel ports, and enable/disable the diskette and enhanced IDE controllers.

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.	
Advanced	
Integrated Peripherals	Item Specific Help
UART1 Port: [3F8h, IRQ 4] UART2 Port: [2F8h, IRQ 3] Parallel Port: [378h, IRQ 7] Parallel Port Mode: [Bi-directional] Diskette controller: [Enabled] Local Bus IDE adapter: [Enabled] UART 2 Mode: [Standard]	If the line item you are viewing has specific help, it will be listed here.

F1 Help	↑↓	Select Item	-/+	Change Values	F9 Setup Defaults
ESC Exit	←→	Select Menu	Enter	Select ▣ Submenu	F10 Previous Values

Option	Description
UART1 Port	Allows the COM port address and IRQ levels to be modified or disabled.
UART2 Port	Allows the COM port address and IRQ levels to be modified or disabled.
Parallel Port	Sets a unique address and interrupt request for the LPT port. "Auto" selects the next available combination. You can choose to disable this option.
Parallel Port Mode	Configures the LPT port. Choices are "Bi-directional" and "Standard Mode."
Diskette Controller	Enables or disables the on-board floppy disk controller.
Local Bus IDE Adapter	Enables or disables the local bus IDE adapter.
UART 2 Mode	Sets the interface to "Standard," "ASKIR," or "IrDA."

Advanced Chipset Control Submenu

Use this menu to change the values in chipset registers and optimize your system's performance.

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.	
Advanced	
Advanced Chipset Control	Item Specific Help
DRAM read timing: [Fast] DRAM write timing: [Fast] I/O recovery time setting: [0 µs] -PCI Features- CPU to PCI write buffer: [Enabled] PCI to DRAM buffer: [Enabled]	If the line item you are viewing has specific help, it will be listed here.

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults

ESC Exit ←→ Select Menu Enter Select ▣ Submenu F10 Previous Values

Option	Description
DRAM read timing	Selects the DRAM read timing speed. Choices are "Slow," "Normal," "Fast," and "Fastest."
DRAM write timing	Selects the DRAM write timing speed. Choices are "Slow," "Normal," "Fast," and "Fastest."
I/O recovery time setting	Sets the minimum time required between back-to-back I/O operations. The default is 0 µs, which allows the system to operate at the fastest rate.
CPU to PCI write buffer	Enables CPU to PCI write buffer feature for improving the CPU to PCI write performance.
PCI to DRAM buffer	Enables PCI to DRAM buffer feature for improving performance.

Note

Leave the options in this menu in their default configurations.

Security Menu

This menu prompts for the new system password and requires you to verify the password by entering it again. The password can be used to stop access to the setup menus or prevent unauthorized booting of the unit. The supervisor password can also be used to change the user password.

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.			
Main	Advanced	Security	Exit
Supervisor Password is	Disabled		Item Specific Help
User Password is	Disabled		If the line item you are viewing has specific help, it will be listed here.
Set Supervisor Password	[Press Enter]		
Set User Password	Press Enter		
Password on boot:	[Disabled]		
Diskette access:	[Supervisor]		
Fixed disk boot sector:	[Normal]		
System backup reminder:	[Disabled]		
Virus check reminder:	[Disabled]		

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults

ESC Exit ←→ Select Menu Enter Select ▣ Submenu F10 Previous Values

Option	Description
Supervisor Password is	Indicates the supervisor password, which is set in the Set Supervisor Password field. If no password is set, this field indicates it is disabled.
User Password is	Indicates the user password, which is set in the Set User Password field. If no password is set, this field indicates it is disabled.
Set Supervisor Password	Provides full access to setup menus. You may use up to seven alphanumeric characters. You can disable the supervisor password by setting this field to "CR" or leaving it empty.
Set User Password	Provides restricted access to setup menus. It requires the prior setting of a supervisor password. You may use up to seven alphanumeric characters. You can disable the user password by setting this field to "CR" or leaving it empty.
Password on Boot	When the supervisor password is set and this option is disabled, BIOS assumes the user is booting.
Diskette Access	Restricts floppy drive access to the supervisor when set to "Supervisor." Requires setting the supervisor password.
Fixed Disk Boot Sector	Write protects the disk boot sector to help prevent viruses.
System Backup Reminder/Virus Check Reminder	When enabled, displays a message during boot up asking (Y/N) if you have backed-up the system or scanned it for any viruses. The message displays each time you boot until you respond with "Y." "Daily" displays the message on the first boot of the day; "Weekly" on the first boot after Sunday; and "Monthly" on the first boot of the month.

Exit Menu

Use this menu to exit the setup menus.

PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.	
Main Advanced Security Exit	
Save Changes & Exit Exit Without Saving Changes Get Default Values Load Previous Values Save Changes	Item Specific Help
	If the item you are viewing has specific help, it will be listed here.

F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
 ESC Exit ←→ Select Menu Enter Select ▣ Submenu F10 Previous Values

Option	Description
Save Changes & Exit	Saves the changes you have made during the current session in battery-backed CMOS RAM, and then exits the setup menus. After you save your selections, the program displays the following message: " Values have been saved." " [Continue]" When you press continue, the system exits the setup menus. The next time you boot your computer, the BIOS configures your system according to the setup selections stored in CMOS. If those values cause the system boot to fail, reboot and press F2 to enter the BIOS setup menus. Once in the setup menus, you can revert to the <u>Default Values</u> (as described below) or change the selections that caused the boot to fail.
Exit Without Saving Changes	Exits the setup menus without storing any new selections you may have made. The previous selections in effect remain in effect.
Get Default Values	Loads the default values for all the Setup menus. After you select this option, the program displays the following message: " Default values have been loaded." " [Continue]" If, during boot up, the BIOS detects a problem with values stored in CMOS, it displays the following messages: " System CMOS checksum bad - run SETUP" " Press <F1> to resume, <F2> to Setup" This indicates that the CMOS values have been corrupted or modified incorrectly. Press F1 to resume the boot (this causes the system to be configured using the default values) or F2 to run the BIOS setup menus with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.
Load Previous Values	Restores the values you previously saved to CMOS if you change your mind about changes you have made and have not yet saved .
Save Changes	Saves all the changes you have made during the current session to battery-backed CMOS RAM, but does not exit the setup menus. You can return to the other menus if you want to review and change your selections.

BIOS Compatibility

This BIOS is IBM PC/AT compatible with additional CMOS RAM and BIOS data areas used.

Appendix A – DRAM Installation

The CHIP4e+ has one 72-pin in-line memory module (SIMM) site in which to add memory. Due to the CPU speed, DRAM access time should be 70 ns or less, and must be 60 ns to run with the fastest memory setting.

The CHIP4e+ can accommodate 4, 8, 16, 32, or 64 Mbytes of DRAM. You may use 1M x 32, 2M x 32, 4M x 32, 8M x 32, and 16M x 32 DRAM SIMM sizes.

Tables A-1 through A-5 list recommended DRAM manufacturers, along with the respective part numbers.

Table 0-13. 1M x 32 Part Numbers (4 Mbytes)

Manufacturer	Part Number	
	Non-EDO	EDO
Micron	MT8D132M-6	MT8D132M-6x
Reptron/PNY	N/A	ME10243208ES-60MT
Siemens	N/A	HYM3210055-60
Xycom	104273	

Table 0-14. 2M x 32 Part Numbers (8 Mbytes)

Manufacturer	Part Number	
	Non-EDO	EDO
Hitachi	N/A	HB56U232SB-6C
Micron	MT6D232M-6	MT6D232M-6x
Reptron/PNY	N/A	ME20483216ES-60MT
Siemens	N/A	HYM322005S-60
Xycom	104258	

Table 0-15. 4M x 32 Part Numbers (16 Mbytes)

Manufacturer	Part Number	
	Non-EDO	EDO
Hitachi	N/A	HB56V832SB-6BN
Micron	MT8D432M-6	MT8D432M-6x
NEC	N/A	MC-42800F32B-60
Xycom	104302	

Table 0-16. 8M x 32 Part Numbers (32 Mbytes)

Manufacturer	Part Number (EDO)
Micron	MT16D832M-6x
Xycom	106054

Table 0-17. 16M x 32 Part Numbers (64 Mbytes)

Manufacturer	Part Number (EDO)
Xycom	123514

Figure 0-1 shows how to install DRAM SIMMS on the CHIP4e+.

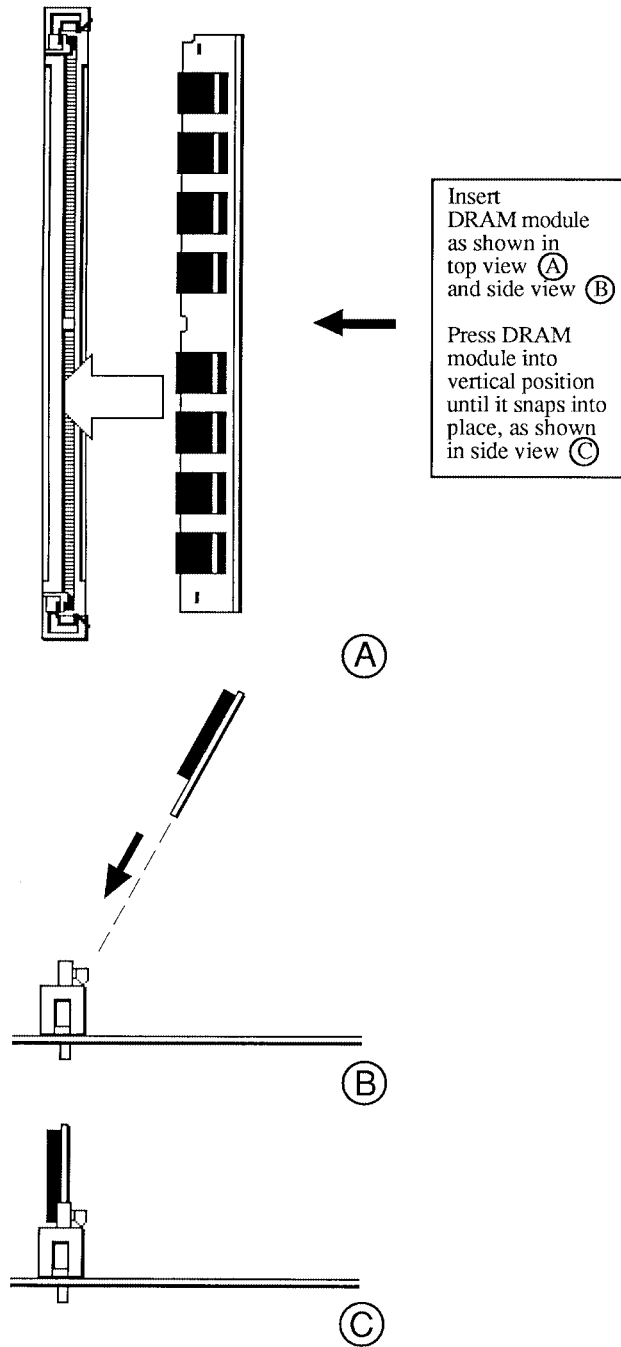


Figure 0-1. DRAM Installation

Appendix B – Video Modes

The Chips & Technologies VGA BIOS supports many standard, VESA, and extended modes. The following tables list the standard and extended video modes, and whether or not they are supported by CRT, TFT active color, and STN passive color displays.

Standard Modes

IBM Mode	VESA Mode	# of Colors	Pixels	Display Mode	CRT	TFT	STN
00	Not Supported	16/256	320x200	text	Supported	Supported	Supported
01	Not Supported	16/256	320x350	text	Supported	Supported	Supported
02	Not Supported	16/256	640x200	text	Supported	Supported	Supported
03	Not Supported	16/256	640x200	text	Supported	Supported	Supported
04	Not Supported	4/256	320x200	graphics	Supported	Supported	Supported
05	Not Supported	4/256	320x200	graphics	Supported	Supported	Supported
06	Not Supported	2/256	640x200	graphics	Supported	Supported	Supported
07	Not Supported	mono	720x350	text	Supported	Supported	Supported
0D	Not Supported	16/256	320x200	graphics	Supported	Supported	Supported
0E	Not Supported	16/256	640x200	graphics	Supported	Supported	Supported
0F	Not Supported	mono	640x350	graphics	Supported	Supported	Supported
10	Not Supported	16/256	640x350	graphics	Supported	Supported	Supported
11,20	Not Supported	2/256	640x480	graphics	Supported	Supported	Supported
12	Not Supported	16/256	640x480	graphics	Supported	Supported	Supported
13	Not Supported	256/256	320x200	graphics	Supported	Supported	Supported

Extended Modes

C&T Mode	VESA Mode	# of Colors	Pixels	Display Mode	CRT	TFT	STN
	100	256	640x400	graphics	Supported	Supported	Supported
30	101	256	640x480	graphics	Supported	Supported	Supported
40	?	32K	640x480	graphics	Supported	Supported	Supported
41	?	64K	640x480	graphics	Supported	Supported	Supported
50	?	16M	640x480	graphics	Supported	Supported	Supported
22	102	16	800x600	graphics	Supported	Not Supported	Not Supported
32	103	256	800x600	graphics	Supported	Not Supported	Not Supported
42	?	32K	800x600	graphics	Supported	Not Supported	Not Supported
43	?	64K	800x600	graphics	Supported	Not Supported	Not Supported
24	104	16	1024x768	graphics	Supported	Not Supported	Not Supported
34	?	256	1024x768	graphics	Supported	Not Supported	Not Supported

Windows[®] 3.1

Windows 3.1 Driver (Version 1.1.1)	CRT	TFT	STN
1024x768x16	Supported	Not Supported	Not Supported
1024x768x256	Supported	Not Supported	Not Supported
1280x1024x16	Not Supported	Not Supported	Not Supported
640x480x16	Supported	Supported	Supported
640x480x256	Supported	Supported	Supported
640x480x32k	Supported	Supported	Supported
640x480x64k	Supported	Supported	Supported
640x480x16M	Supported	Supported	Supported
800x600x16	Supported	Not Supported	Not Supported
800x600x256	Supported	Not Supported	Not Supported
800x600x32k	Supported	Not Supported	Not Supported
800x600x64k	Supported	Not Supported	Not Supported

Note

All Windows' drivers were tested on a NEC multisync 5FG monitor.

Windows 95

Windows 95 Driver (Version 4.0)	CRT
1024x768x256	Supported
640x480x16	Supported
640x480x256	Supported
640x480x16bit	Supported
640x480x24bit	Supported
800x600x16	Supported
800x600x256	Supported
800x600x16bit	Supported

Windows NT® 3.5

Windows NT Driver (Version 1.1.0)	CRT
1024x768x256	Supported
640x480x256	Supported
640x480x64k	Supported
800x600x256	Supported
800x600x64k	Supported

Note

All rates tested and passed on NEC multisync 5FG monitor except 30 Hz modes (not supported by monitor).

OS/2 Warp 3

OS/2 Warp Driver (Version 1.1.0)	CRT
1024x768x256	Supported
640x480x256	Supported
640x480x64k	Supported
640x480x16M	Supported
800x600x256	Supported

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